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01/21/2003

1 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:430624 HCAPLUS
DN 131:52793
TI Differential gate oxide thickness by nitrogen implantation for mixed mode and embedded VLSI circuits
IN Sun, Shih-wei; Tsai, Meng-jin
PA United Microelectronics Corp., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5920779	A	19990706	US 1997-903595	19970731 <--
PRAI	US 1997-47252P	P	19970521		

AB Different thicknesses of gate oxide can be formed on a single chip in a single oxidn. process by selectively implanting N into the surface of the chip in a pattern corresponding to the desired differences in gate oxide thickness. Implanting N in a Si substrate reduces the rate at which oxide grows on the surface. Thus, by implanting different dosages of N into the surface of the substrate, thicker or thinner oxide layers can be provided. A processing chip with embedded DRAM can then be formed in which the logic circuitry has a thin gate oxide and the DRAM circuitry has a thick gate oxide by implanting the higher dosage of N into the region of the chip where the logic circuits are to be formed. Different gate oxide thicknesses are then provided by exposing both the logic circuitry and the embedded DRAM section to a single thermal oxidn. process.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:392905 HCAPLUS
DN 131:66693
TI Metal-metal capacitors for DRAM and fabrication thereof
IN Lee, Kuo-Hua
PA Lucent Technology Inc., USA
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11168189	A2	19990622	JP 1998-262181	19980917 <--
PRAI	US 1997-932005		19970917		

AB The title capacitors are provided by (1) depositing a 1st oxide layer in a horizontal position above a conductive window and a metallic region in contact to source/drain in a transistor, (2) forming a window in the 1st oxide layer, (3) forming a conductive plug in the window, (4) forming a 1st pattern for a coupler between the conductive plugs or memory cell bit lines on the 1st oxide layer, (4) depositing a 2nd oxide layer over the pattern region, and (5) forming a conductive plug in the window. The formation of the capacitors in horizontal position makes CMP process more effective in the manufg. process.

L16 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:435793 HCAPLUS
DN 129:102998
TI Fabrication of semiconductor device, especially plug protection process for use in the manufacture of embedded dynamic random access memory (DRAM)

01/21/2003

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     cells
IN   Jiang, Bo; Zurcher, Peter; Jones, Robert E.; White, Bruce E.
PA   Motorola, Inc., USA
SO   U.S., 11 pp.
     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.       KIND  DATE          APPLICATION NO.   DATE
     ---------------  ----  --------      ---------------   --------
PI   US 5773314        A    19980630      US 1997-845457    19970425 <--
     JP 10303398       A2   19981113      JP 1998-125234    19980420 <--
PRAI US 1997-845457         19970425
AB   A method for forming an embedded DRAM structure along with tungsten
     plugged MOS transistor devices begins by forming capacitor tungsten plugs
     and bit-line tungsten plugs.  A bottom capacitor electrode is formed to
     protect the tungsten plug.  Simultaneously, an optionally-removable
     barrier region is formed to protect the plug.  A capacitor dielec. is
     deposited and oxygen annealed to form a ferroelec. capacitor material.
     The barrier and the lower electrode protect all of the tungsten plugs from
     being adversely oxidized by the oxygen anneal.  A top electrode of the
     ferroelec. capacitor is then deposited, lithog. patterned, and etched.
     The lithog. patterning and etching of the top electrode may also be
     further utilized to remove the barrier region.
RE.CNT  10     THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16  ANSWER 4 OF 9  WPIX (C) 2003 THOMSON DERWENT
AN   2002-223831 [28]   WPIX
DNN  N2002-171300       DNC C2002-068333
TI   Fabrication of self-aligned contact in an embedded dynamic random access
     memory involves forming a dielectric layer and contact holes in memory and
     logic regions of a substrate until source/drain regions are exposed.
DC   L03 U11 U12 U13
IN   CHEN, J; LIN, Y
PA   (UNMI-N) UNITED MICROELECTRONICS CORP
CYC  1
PI   US 6200848    B1 20010313 (200228)*      11p <--
ADT  US 6200848 B1 US 1998-208612 19981208
PRAI US 1998-208612   19981208
AB   US    6200848 B UPAB: 20020502
     NOVELTY - Metal oxide semiconductors and source/drain regions are formed
     in memory and logic regions of a substrate. Dielectric layer and contact
     holes are formed in memory and logic regions until source/drain regions
     are exposed. Silicide layers are formed over contact holes and an
     interlayer dielectric is formed. Conductive vias are formed in memory and
     logic regions, and self-aligned contact is formed.
          DETAILED DESCRIPTION - Fabricating a self-aligned contact, where a
     substrate (500) having a memory region (504) and a logic region (506) is
     provided, and metal oxide semiconductors (MOS) are respectively formed in
     the memory region (504) and in the logic region (506), comprises:
          (a) forming as defined dielectric layer on the substrate (500);
          (b) forming a first contact hole (522a) in the dielectric layer in
     the memory region, and simultaneously forming a second contact hole (522b)
     in the logic region until the substrate (500) is exposed;
          (c) forming a first silicide layer (524a) over the first contact hole
     (522a) and a second silicide layer (524b) over the second contact hole
     (522b), respectively, to couple electrically the first and second silicide
     layers (524a, 524b) to the substrate (500), where portions of the first
     and second silicide layers (524a, 524b) extend to the surface of the
     dielectric layer neighboring the first and second contact holes;
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(d) forming a defined interlayer dielectric (526) over the substrate (500);

(e) forming a first via in the logic region (506) to expose the first silicide layer (524a) and a second via in the memory region (504) until the second silicide layer (524b) is exposed; and

(f) forming a first metal (preferably tungsten) plug in the first via and a second metal plug in the second via, respectively, to couple the first and second silicide layers.

The first and second silicide layers (524a, 524b) can be titanium silicide or they can be cobalt silicide, and they are formed by a sputtering or chemical vapor deposition process.

USE - Dynamic random access memory manufacture.

ADVANTAGE - The invention overcomes the difficulties of forming and aligning a contact hole, because the thickness of dielectric layers in a memory region and in a logic region are very different.

DESCRIPTION OF DRAWING(S) - The drawing show a cross-sectional view of a self-aligned contact formed in an embedded DRAM, according to an embodiment of the invention.

Semiconductor substrate 500
Shallow trench isolation structure 502
Memory region 504
Logic region 506
Gate structure 508
Source/drain regions 510, 514
Dual gate structure 512
Oxide layer 516
Hard material layer 518
Dielectric layer 520
Contact holes 522a, 522b
Patterned silicide layers 524a, 524b
Interlayer dielectric layer 526
Metal plugs 528a, 528b
Dwg.5D/5

L16 ANSWER 5 OF 9 WPIX (C) 2003 THOMSON DERWENT
AN 1999-394747 [33] WPIX
DNN N1999-295069 DNC C1999-115951
TI Manufacture of integrated circuit devices such as high speed processing circuits, embedded circuits e.g. embedded DRAMs, mixed mode circuits and other circuits incorporating FETs.
DC L03 U11 U13
IN SUN, S; TSAI, M
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 5920779 A 19990706 (199933)* 13p <--
ADT US 5920779 A Provisional US 1997-47252P 19970521, US 1997-903595 19970731
PRAI US 1997-47252P 19970521; US 1997-903595 19970731
AB US 5920779 A UPAB: 19990819

NOVELTY - Different thicknesses of gate oxide (46) are formed on a single chip.

DETAILED DESCRIPTION - Forming an IC device comprises:

(a) providing a semiconductor substrate (10) with first and second regions on which MOS devices are to be formed;

(b) masking the second region and providing a first concentration of a first dopant in the substrate at the surface of the first region without doping the second region;

(c) removing the mask over the second region;

(d) masking the first region and providing a second concentration of a second dopant in the substrate at the surface of the second region without doping the first region;

(e) oxidizing (46) the surface of the substrate to grow a first

thickness of oxide on the first region of the substrate and growing a second, different thickness of oxide on the second region in a single oxidizing process; and

(f) forming MOS devices on the two regions.

USE - Manufacture of integrated circuit devices such as high speed processing circuits, embedded circuits e.g. embedded DRAMs, mixed mode circuits and other circuits incorporating FETs with different thicknesses of gate oxides on a single chip.

ADVANTAGE - The substrate is subjected to only one high temperature oxidation step therefore the process is simplified and shortened.

DESCRIPTION OF DRAWING(S) - The drawing shows a processing circuit with embedded DRAM incorporating different thicknesses of gate oxide.

Substrate 10

Gate oxide layer 46

Capacitor electrodes 102,104,108

Dwg.6c/6

L16 ANSWER 6 OF 9 WPIX (C) 2003 THOMSON DERWENT
AN 1999-312339 [26] WPIX
DNN N1999-233274 DNC C1999-092159
TI Dynamic random access memory (DRAM) device having metal-to-metal capacitor.
DC L03 U12 U13 U14
IN LEE, G H; LEE, K
PA (LUCE) LUCENT TECHNOLOGIES INC
CYC 3

PI	US 5903493	A	19990511	(199926)*	11p	<--
	JP 11168189	A	19990622	(199935)	9p	<--
	KR 99029975	A	19990426	(200028)		<--

ADT US 5903493 A US 1997-932005 19970917; JP 11168189 A JP 1998-262181 19980917; KR 99029975 A KR 1998-38910 19980916
PRAI US 1997-932005 19970917
AB US 5903493 A UPAB: 19990723

NOVELTY - A DRAM comprises a planarized oxide, having a patterned metal region M1, on a substrate containing a transistor. At least one capacitor (12) is formed within the oxide between M1 and the upper oxide surface and includes planarized lower and upper plates (22,26) and a planarized dielectric (24).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a DRAM as above comprising four successive planarized oxide layers with M1 between the first two and the capacitor between the second and third oxide layers.

USE - As capacitors for storage cells in DRAMs

ADVANTAGE - The device is made by a method which is more compatible with existing fabrication processes than conventional etching, i.e., chemical-mechanical polishing can be used and planarization is maintained.

DESCRIPTION OF DRAWING(S) - A cross-section of the metal-to-metal DRAM capacitor is shown.

Capacitor 12

Lower and upper electrodes 22,26

Dielectric 24

Dwg.1/8

L16 ANSWER 7 OF 9 WPIX (C) 2003 THOMSON DERWENT
AN 1998-387021 [33] WPIX
DNN N1998-301805 DNC C1998-116994
TI Embedded dynamic random access memory (DRAM) cells - fabricated using protection of metallic transistor contact plugs from the oxygen annealing of high dielectric constant dielectric capacitors.
DC L03 U11 U12 U13 U14
IN JIANG, B; JONES, R E; WHITE, B E; ZURCHER, P

01/21/2003

PA (MOTI) MOTOROLA INC
CYC 2
PI US 5773314 A 19980630 (199833)* 11p <--
JP 10303398 A 19981113 (199905) 10p <--
ADT US 5773314 A US 1997-845457 19970425; JP 10303398 A JP 1998-125234 19980420
PRAI US 1997-845457 19970425
AB US 5773314 A UPAB: 19980819
A DRAM embedded structure with tungsten plugged MOS transistor devices is fabricated by; forming tungsten plugs (46) and bit line tungsten plugs (44) with a bottom capacitor electrode (48b) to protect the plug (46). Simultaneously an optionally removable barrier region (48a) is formed to protect the bit line plug (44). Capacitor dielectric (52) is deposited and oxygen annealed to form a ferroelectric capacitor material when the barrier (48a) and the lower electrode (48b) protect the tungsten plugs from oxidation. A top electrode layer (54,56) is then deposited, patterned , and etched when the barrier (48a) is removed. Interlayer dielectric (58) and contact plugs (60) are then formed to complete the structure. The barrier and bottom electrode (48a,b) are typically sputter deposited iridium which is etched using ion milling

USE - Fabrication of embedded DRAMs.

ADVANTAGE - Embedded ferroelectric DRAM capacitors which require an oxygen anneal can be achieved without oxidation of the tungsten metal plugs.

Dwg.7/8

L16 ANSWER 8 OF 9 JAPIO COPYRIGHT 2003 JPO
AN 1999-168189 JAPIO
TI METAL-TO-METAL CAPACITOR DEVICE AND MANUFACTURE THEREOF
IN LEE KUO-HUA
PA LUCENT TECHNOL INC
PI **JP 11168189** A 19990622 Heisei
AI JP 1998-262181 (JP10262181 Heisei) 19980917
PRAI US 1997-932005 19970917
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To reconcile the production process of a DRAM(dynamic random access memory) with the existing production process of the DRAM by a method wherein the DRAM is produced by a method wherein first to third oxide layers are deposited and with windows and conductive plugs formed in the oxide layers, a metal regions is formed on each oxide layer and thereafter, a fourth flattened oxide layer is deposited.
SOLUTION: A planarized oxide region or a layer 52 is formed on a substrate 16. Windows 54 are formed in the layer 52, the windows 54 are filled with a proper conductive material and conductive plugs are formed in the windows. A metal region 28 formed by patterning exists on the flattened oxide layer 52. Another planarized oxide region or layer 56 exists on the layer 52 and the region 28 formed through by patterning. The planarized oxide layer 56 has windows/plug regions 58 in the interior thereof. Metal regions 61 formed by patterning respectively exist on capacitors 12. Moreover, another planarized oxide region or layer 63 exists on the layer 56, the capacitors 12 and the regions 61 have windows/plug regions 65 in the interior thereof. The last planarized oxide region or layer 69 exists on the layer 63 and regions 67.
COPYRIGHT: (C)1999,JPO

L16 ANSWER 9 OF 9 JAPIO COPYRIGHT 2003 JPO
AN 1998-303398 JAPIO
TI METHOD FOR FORMING SEMICONDUCTOR DEVICE
IN JIANG BO; ZURCHER PETER; JONES ROBERT E; WHITE BRUCE E
PA MOTOROLA INC
PI **JP 10303398** A 19981113 Heisei

01/21/2003

AI JP 1998-125234 (JP10125234 Heisei) 19980420
PRAI US 1997-845457 19970425
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To enable the integration of ferroelectric device of on-chip with an MOS logic including a tungsten plug.
SOLUTION: Concerning a method for forming integrated DRAM structure together with the MOS transistor device of tungsten plug system, first of all, a capacitor tungsten plug 46 and a bit line tungsten plug 44 are former. Next, the tungsten plug 46 is protected by forming a bottom capacitor electrode 48b. At the same time, an arbitrarily selectively removable barrier area is formed for protecting the plug 44. Ferroelectric capacitor materials are formed by coating and oxygen-annealing the capacitor dielectric 52. The barrier area and a lower electrode 48b protect all the tungsten plugs 46 and 44 from being oxidized by oxygen annealing. Next, head electrodes 54 and 56 of ferroelectric capacitor are attached, lithographically patterned and etched.

01/21/2003

L21 ANSWER 1 OF 4 WPIX (C) 2003 THOMSON DERWENT
AN 2002-426360 [45] WPIX
DNN N2002-335249 DNC C2002-120884
TI Top oxide layer protecting process in vertical MOSFET DRAM arrays, involves depositing thin polysilicon or amorphous layer over top oxide layer.
DC L03 U11
IN DIVAKARUNI, R; JAIPRAKASH, V; MALIK, R; MANDELMAN, J; SEITZ, M
PA (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 21
PI WO 2002031878 A2 20020418 (200245)* EN 13p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR
ADT WO 2002031878 A2 WO 2001-US26644 20010824
PRAI US 2000-670741 20000927
AB WO 200231878 A UPAB: 20020717

NOVELTY - An array **gate conductor** (GC) polysilicon layer (17) of a vertical MOSFET is planarized to the top surface of a top oxide layer (16). A thin polysilicon or amorphous silicon layer (18) which serves as a silicon nitride etch stop layer, is deposited on the top oxide layer.

DETAILED DESCRIPTION - An active area (AA) pad nitride layer and a tetraethyl orthosilicate (TEOS) stack layer are deposited on the thin polysilicon or amorphous silicon layer. The AA mask pad layer is opened to the silicon surface of a substrate for forming an isolation trench. The isolation trench filled with a high density plasma (HDP) oxide material and planarized to the top surface of the AA pad nitride layer. The AA pad nitride layer is stripped with the thin polysilicon or amorphous silicon layer which serves as an etch stop layer to protect the underlying top oxide layer. An etch support (ES) mask is patterned to open the support areas and to etch the ES nitride, thin polysilicon layer and top oxide layer from exposed areas. An etch array (EA) mask is used to open the support gate polysilicon in the array and for removing the selective ES nitride layer underlying polysilicon layer for protecting the top oxide layer.

USE - For protecting top oxide layer during manufacture of integrated circuit such as vertical metal oxide semiconductor field effect transistor (**MOSFET**) **dynamic random access memory** (DRAM) arrays.

ADVANTAGE - The thin polysilicon or amorphous silicon layer serves as a silicon nitride etch stop layer and effectively protects the underlying top oxide layer from etch damage.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a thin polysilicon layer or amorphous silicon layer deposited following array gate chemical-mechanical polish (CMP) to the top surface of the top oxide layer and following the formation of isolation trenches.

Top oxide layer 16
Array **gate conductor** polysilicon layer 17
Polysilicon or amorphous silicon layer 18
Dwg.1/5

L21 ANSWER 2 OF 4 WPIX (C) 2003 THOMSON DERWENT
AN 2002-507418 [54] WPIX
CR 2002-214352 [27]
DNN N2002-401538 DNC C2002-144235
TI Formation of dual work function **metal oxide semiconductor** field effect **transistor/embedded dynamic random access memory** array by removing exposed second polysilicon layer while removing exposed

portions of first polysilicon layer.
DC L03 U11 U12 U14
IN DIVAKARUNI, R; MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 2002055224 A1 20020509 (200254)* 24p
ADT US 2002055224 A1 Div ex US 2000-706492 20001103, US 2001-862827 20010522
PRAI US 2000-706492 20001103; US 2001-862827 20010522
AB US2002055224 A UPAB: 20020823

NOVELTY - A dual work function high performance **metal oxide semiconductor** field effect **transistor/ embedded dynamic random access memory** array is formed by removing an exposed second polysilicon layer from an isolation region, while simultaneously removing exposed portions of a first polysilicon layer in a support region(S) in which a **gate conductor** guard ring is formed on the isolation region.

DETAILED DESCRIPTION - Formation of a dual workfunction high performance **metal oxide semiconductor** field effect **transistor/embedded dynamic random access memory** (**MOSFET/ EDRAM**) array having a **gate conductor** (30) guard ring formed around the array region, comprises providing a memory structure having an array region(s) and a support region(s) which are separated by an isolation region (16). The array region(s) includes DRAM cells embedded in a substrate (18). Adjacent DRAM cells are connected to each other through bitline diffusion regions (22) which are capped with an oxide capping layer (44). A patterned nitride layer is formed on all exposed surfaces in the array region(s) and on a portion of the isolation region. A gate oxide is formed on the substrate in the support region(s). A stack comprising a first polysilicon layer (42) and a dielectric capping layer (56) is formed on all exposed surfaces of the memory structure. The dielectric capping layer, the first polysilicon layer, and the nitride layer are removed from the array region(s). Wordlines (52) are formed on the DRAM cells in the array region(s). Spacers (58) are formed on exposed sidewalls of the wordlines, and on exposed sidewalls of the stack remaining in the structure. A block mask is formed on a support region(s) and a portion of the DRAM cells that is adjacent to the isolation region. It does not cover the oxide capping layer. The oxide capping layer on the bitline diffusion regions is removed, and the block mask is stripped. A patterned second polysilicon layer is formed on the array region and the stack which is present on the isolation region. The dielectric capping layer is removed in the support region(s). A doped glass material layer is formed on all surfaces in the array region(s) and the support region(s). The doped glass material layer is patterned to form hard masks in the array region(s) and the support region(s). The hard mask in the array region(s) defines a bitline of the memory structure, and the hard mask in the support region(s) defines a support gate region. The exposed second polysilicon layer is removed from the array region(s) and the isolation region, while simultaneously removing exposed portions of the first polysilicon layer in the support region(s) in which a **gate conductor** guard ring is formed on the isolation region, and the support gate region is formed in the support region(s). The hard masks are removed from an array region(s) and the support region(s), and a screen oxide layer (66) is formed on any exposed silicon surfaces. Source and drain regions (74) are formed on the support gate region(s). An oxide overlying the bitline, support gate region, and source and drain regions, is removed to expose silicon surfaces. The exposed silicon surfaces are salicided to provide salicide regions (76) on the bitline, the gate region and the source and drain regions.

USE - For the formation of dual workfunction high performance

MOSFET/EDRAM.
ADVANTAGE - The method eliminates additional masking steps to form high performance complementary metal oxide semiconductor logic devices and borderless contacts. It does not share support **gate conductor** lithography with wordline lithography. It shares the **gate conductor** lithography with the array bitline lithography step. The presence of the guard ring provides an internal protection scheme, which prevents the designer from placing **gate conductor** across the isolation region.
DESCRIPTION OF DRAWING(S) - The figure shows a pictorial view of the processing step of the inventive method.
Isolation region 16
Substrate 18
Bitline diffusion regions 22
Gate conductor 30
Oxide capping layer 44
First polysilicon layer 42
Wordlines 52
Conductive metal 54
Dielectric capping layer 56
Spacers 58
Screen oxide layer 66
Source and drain regions 74
Salicide regions 76
Dwg.12/27

L21 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2003 ACS DUPLICATE 1
AN 2001:521838 HCAPLUS
DN 135:85641
TI Method for forming dual work function high-performance support MOSFETs in EDRAM arrays
IN Mandelman, Jack A.; Divakaruni, Ramachandra; Radens, Carl J.
PA International Business Machines Corp., USA
SO U.S., 23 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6261894	B1	20010717	US 2000-706492	20001103
PRAI	US 2000-706492		20001103		

AB Methods of prepg. dual work function high-performance support metal oxide semiconductor field effect transistor (MOSFETs)/embedded dynamic random access (EDRAM) arrays are provided. The methods describe herein reduce the no. of deep-UV masks used in the forming memory structure, decouple the support and arraying processing steps, provide salicided gates, source/drain regions and bitlines, and provide, in some instances, local interconnects at no addnl. processing costs. Dual work function high-performance support **MOSFETs/EDRAM** arrays having a **gate conductor** guard ring and/or local interconnections are also provided.
RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L21 ANSWER 4 OF 4 WPIX (C) 2003 THOMSON DERWENT
AN 2002-235019 [29] WPIX
DNN N2002-180351 DNC C2002-071342
TI Method of manufacturing memory cell involves forming trench capacitor by etching filler material, substrate and polysilicon layer and replacing filler material with place holder material, at location corresponding to

wordline **gate conductor**.
DC L03 U11
IN FURUKAWA, T; MANDELMAN, J A; TONTI, W R
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6271080 B1 20010807 (200229)* 41p
ADT US 6271080 B1 US 1999-465109 19991216
PRAI US 1999-465109 19991216
AB US 6271080 B UPAB: 20020508
NOVELTY - Memory cell fabrication method involves forming trench capacitor by etching filler material, substrate and polysilicon layer and then replacing filler material with place holder material, at location corresponding to wordline **gate conductor**.

DETAILED DESCRIPTION - A stack including a pad oxide layer, nitride pad layer, oxide layer and polysilicon layer is formed on a substrate. The stack is etched at preset locations and filled with filler material such as oxide. The trench capacitors are formed in the substrate by etching filler material, substrate and polysilicon layer. Then polysilicon layer and a portion of oxide layer are planarized. The portion of stack or filler material is replaced with place holder material at location corresponding to wordline **gate conductor** (42), for forming **gate conductor**.

USE - The method is used for fabricating memory cell such as 8F2 planar metal oxide semiconductor field effect transistor (**MOSFET**) **dynamic random access memory** (DRAM) cell.

ADVANTAGE - Eliminates wordline **gate conductor** to storage trench overlay sensitivity problem effectively.

DESCRIPTION OF DRAWING(S) - The figure shows fabrication process of 8F2 planar MOSFET DRAM cell.

Wordline **gate conductor** 42
Dwg.15/29

01/21/2003

L27 ANSWER 1 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:540209 HCAPLUS
DN 137:87118
TI EDRAM cell with double-gated vertical MOSFET and self-aligned STI
IN Mandelman, Jack A.; Divakaruni, Ramachandra; Radens, Carl J.; Bronner, Gary B.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 24 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002094619	A1	20020718	US 2001-766013	20010118
PRAI	US 2001-766013		20010118		

AB The invention relates to a process for making a memory cell contg. double-gated vertical metal oxide semiconductor field effect transistors (MOSFET) and isolation regions such as shallow trench isolation, STI, regions that are self-aligned to the word lines and bit lines of the cell are provided. Said memory cell substantially eliminates the back-gating problem and floating well effects that are typically present in prior art memory cells.

L27 ANSWER 2 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-426360 [45] WPIX
DNN N2002-335249 DNC C2002-120884
TI Top oxide layer protecting process in vertical MOSFET DRAM arrays, involves depositing thin **polysilicon** or amorphous layer over top oxide layer.
DC L03 U11
IN DIVAKARUNI, R; JAIPRAKASH, V; MALIK, R; MANDELMAN, J; SEITZ, M
PA (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 21
PI WO 2002031878 A2 20020418 (200245)* EN 13p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR
ADT WO 2002031878 A2 WO 2001-US26644 20010824
PRAI US 2000-670741 20000927
AB WO 200231878 A UPAB: 20020717
NOVELTY - An array gate conductor (GC) **polysilicon** layer (17) of a vertical MOSFET is planarized to the top surface of a top oxide layer (16). A thin **polysilicon** or amorphous **silicon** layer (18) which serves as a **silicon** nitride etch stop layer, is deposited on the top oxide layer.

DETAILED DESCRIPTION - An active area (AA) pad nitride layer and a tetraethyl orthosilicate (TEOS) stack layer are deposited on the thin **polysilicon** or amorphous **silicon** layer. The AA mask pad layer is opened to the **silicon** surface of a substrate for forming an isolation trench. The isolation trench filled with a high density plasma (HDP) oxide material and planarized to the top surface of the AA pad nitride layer. The AA pad nitride layer is stripped with the thin **polysilicon** or amorphous **silicon** layer which serves as an etch stop layer to protect the underlying top oxide layer. An etch support (ES) mask is patterned to open the support areas and to etch the ES nitride, thin **polysilicon** layer and top oxide layer from exposed areas. An etch array (EA) mask is used to open the support gate **polysilicon** in the array and for removing the selective ES nitride layer underlying **polysilicon** layer for protecting the top oxide

layer.
USE - For protecting top oxide layer during manufacture of integrated circuit such as vertical metal oxide semiconductor field effect transistor (**MOSFET**) **dynamic random access memory** (DRAM) arrays.
ADVANTAGE - The thin **polysilicon** or amorphous **silicon** layer serves as a **silicon** nitride etch stop layer and effectively protects the underlying top oxide layer from etch damage.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a thin **polysilicon** layer or amorphous **silicon** layer deposited following array gate chemical-mechanical polish (CMP) to the top surface of the top oxide layer and following the formation of isolation trenches.
Top oxide layer 16
Array gate conductor **polysilicon** layer 17
Polysilicon or amorphous **silicon** layer 18
Dwg.1/5

L27 ANSWER 3 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-507418 [54] WPIX
CR 2002-214352 [27]
DNN N2002-401538 DNC C2002-144235
TI Formation of dual work function **metal oxide semiconductor** field effect **transistor/embedded dynamic random access memory** array by removing exposed second **polysilicon** layer while removing exposed portions of first **polysilicon** layer.
DC L03 U11 U12 U14
IN DIVAKARUNI, R; MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 2002055224 A1 20020509 (200254)* 24p
ADT US 2002055224 A1 Div ex US 2000-706492 20001103, US 2001-862827 20010522
PRAI US 2000-706492 20001103; US 2001-862827 20010522
AB US2002055224 A UPAB: 20020823
NOVELTY - A dual work function high performance **metal oxide semiconductor** field effect **transistor/ embedded dynamic random access memory** array is formed by removing an exposed second **polysilicon** layer from an isolation region, while simultaneously removing exposed portions of a first **polysilicon** layer in a support region(S) in which a gate conductor guard ring is formed on the isolation region.
DETAILED DESCRIPTION - Formation of a dual workfunction high performance **metal oxide semiconductor** field effect **transistor/embedded dynamic random access memory** (**MOSFET/ EDRAM**) array having a gate conductor (30) guard ring formed around the array region, comprises providing a memory structure having an array region(s) and a support region(s) which are separated by an isolation region (16). The array region(s) includes DRAM cells embedded in a substrate (18). Adjacent DRAM cells are connected to each other through bitline diffusion regions (22) which are capped with an oxide capping layer (44). A patterned nitride layer is formed on all exposed surfaces in the array region(s) and on a portion of the isolation region. A gate oxide is formed on the substrate in the support region(s). A stack comprising a first **polysilicon** layer (42) and a dielectric capping layer (56) is formed on all exposed surfaces of the memory structure. The dielectric capping layer, the first **polysilicon** layer, and the nitride layer are removed from the array region(s). Wordlines (52) are formed on

the DRAM cells in the array region(s). Spacers (58) are formed on exposed sidewalls of the wordlines, and on exposed sidewalls of the stack remaining in the structure. A block mask is formed on a support region(s) and a portion of the DRAM cells that is adjacent to the isolation region. It does not cover the oxide capping layer. The oxide capping layer on the bitline diffusion regions is removed, and the block mask is stripped. A patterned second **polysilicon** layer is formed on the array region and the stack which is present on the isolation region. The dielectric capping layer is removed in the support region(s). A doped glass material layer is formed on all surfaces in the array region(s) and the support region(s). The doped glass material layer is patterned to form hard masks in the array region(s) and the support region(s). The hard mask in the array region(s) defines a bitline of the memory structure, and the hard mask in the support region(s) defines a support gate region. The exposed second **polysilicon** layer is removed from the array region(s) and the isolation region, while simultaneously removing exposed portions of the first **polysilicon** layer in the support region(s) in which a gate conductor guard ring is formed on the isolation region, and the support gate region is formed in the support region(s). The hard masks are removed from an array region(s) and the support region(s), and a screen oxide layer (66) is formed on any exposed **silicon** surfaces. Source and drain regions (74) are formed on the support gate region(s). An oxide overlying the bitline, support gate region, and source and drain regions, is removed to expose **silicon** surfaces. The exposed **silicon** surfaces are salicided to provide salicide regions (76) on the bitline, the gate region and the source and drain regions.

USE - For the formation of dual workfunction high performance **MOSFET/EDRAM**.

ADVANTAGE - The method eliminates additional masking steps to form high performance complementary metal oxide semiconductor logic devices and borderless contacts. It does not share support gate conductor lithography with wordline lithography. It shares the gate conductor lithography with the array bitline lithography step. The presence of the guard ring provides an internal protection scheme, which prevents the designer from placing gate conductor across the isolation region.

DESCRIPTION OF DRAWING(S) - The figure shows a pictorial view of the processing step of the inventive method.

Isolation region 16
Substrate 18
Bitline diffusion regions 22
Gate conductor 30
Oxide capping layer 44
First **polysilicon** layer 42
Wordlines 52
Conductive metal 54
Dielectric capping layer 56
Spacers 58
Screen oxide layer 66
Source and drain regions 74
Salicide regions 76
Dwg.12/27

L27 ANSWER 4 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-681135 [73] WPIX
DNN N2002-537615 DNC C2002-192145
TI Memory array and support transistor formation on semiconductor substrate comprises forming silicide layers on source/drain regions and on **polysilicon** layer overlying bitline diffusion regions and defining landing pad.
DC L03 U11 U12 U13 U14
IN DIVAKARUNI, R; GRUENING, U; MANDELMAN, J A; NESBIT, L; RADENS, C

01/21/2003

PA (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6429068 B1 20020806 (200273)* 18p
ADT US 6429068 B1 US 2001-897868 20010702
PRAI US 2001-897868 20010702
AB US 6429068 B UPAB: 20021113

NOVELTY - Forming a memory array and support transistors on a semiconductor substrate comprises simultaneously forming silicide layers on an exposed portion of source and drain regions in the support region, on the second **polysilicon** layer overlying bitline diffusion regions in the array region, and on the second **polysilicon** layer defining a landing pad.

DETAILED DESCRIPTION - Forming a memory array and support transistors on a semiconductor substrate (202) comprises providing a memory structure having an array region and a support region separated by an isolation region (208). The array region includes dynamic random access memory cells embedded in the substrate. Adjacent random access memory cells are connected to each other through bitline diffusion regions (214). The memory structure is capped with a top oxide layer (210). A block mask is applied to protect the array region while stripping the top oxide layer from the support region. Support implants and a support gate oxide layer are formed. A first **polysilicon** layer (302) is patterned onto the support gate oxide layer. A conductive nitride barrier layer (250), a metal layer (252) and a dielectric capping layer (254) are formed on all exposed surfaces of the substrate. Portions of the nitride barrier layer, metal layer and dielectric capping layer are removed from the support region to form a support gate structure. The nitride barrier layer, metal layer and dielectric capping layer are removed from the isolation region. The support gate structure comprises the gate oxide layer, first **polysilicon** layer, nitride barrier layer, metal layer, and dielectric capping layer. An insulated spacer is formed on sidewalls of the gate structure. A protective layer is formed on all exposed surfaces of the substrate. An array gate structure is formed in contact with the memory cell. A portion of the bitline diffusion region is exposed by removing portions of the protective layer, the nitride barrier layer, the metal layer and the dielectric capping layer from the array region. The array gate structure comprises the oxide layer, the nitride barrier layer, the metal layer and the dielectric capping layer. The protective layer is simultaneously removed from the isolation region. A spacer layer is formed on sidewalls of the array gate structure. A second **polysilicon** layer is deposited onto the substrate. It is selectively patterned and etched in the isolation region to form a landing pad while the **polysilicon** layer is removed from the support regions. Silicide layers are simultaneously formed on an exposed portion of the source and drain regions in the support region, on the second **polysilicon** layer overlying the bitline diffusion regions in the array region, and on the second **polysilicon** layer defining the landing pad.

USE - For the production of embedded vertical **MOSFET dynamic random access memory** (DRAM) cells.

ADVANTAGE - The process eliminates the need for a metallization layer which is the most difficult layer to photolithographically pattern. Reliance on complicated optical proximity correction schemes and alternating phase shift masking techniques is reduced.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional view illustrating the production of a DRAM array and supports.

Substrate 202
Isolation region 208
Top oxide layer 210
Bitline diffusion regions 214

Nitride barrier layer 250
Metal layer 252
Dielectric capping layer 254
Polysilicon layer 302
Dwg.10/10

L27 ANSWER 5 OF 24 HCAPLUS COPYRIGHT 2003 ACS DUPLICATE 1
AN 2001:521838 HCAPLUS
DN 135:85641
TI Method for forming dual work function high-performance support MOSFETs in EDRAM arrays
IN Mandelman, Jack A.; Divakaruni, Ramachandra; Radens, Carl J.
PA International Business Machines Corp., USA
SO U.S., 23 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6261894	B1	20010717	US 2000-706492	20001103
PRAI	US 2000-706492		20001103		

AB Methods of prepg. dual work function high-performance support metal oxide semiconductor field effect transistor (MOSFETs)/embedded dynamic random access (EDRAM) arrays are provided. The methods describe herein reduce the no. of deep-UV masks used in the forming memory structure, decouple the support and arraying processing steps, provide salicided gates, source/drain regions and bitlines, and provide, in some instances, local interconnects at no addnl. processing costs. Dual work function high-performance support **MOSFETs/EDRAM** arrays having a gate conductor guard ring and/or local interconnections are also provided.
RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 6 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2001-496391 [54] WPIX
DNN N2001-367859 DNC C2001-148993
TI Manufacture of array and support structures for semiconductor devices, e.g. metal oxide semiconductor field effect transistors, involves forming simultaneously first oxide in V-groove surface and second oxide in planar surface.
DC L03 U11
IN FURUKAWA, T; GAMBINO, J P; KIEWRA, E W; MANDELMAN, J A; RADENS, C J; TONTI, W R; WEYBRIGHT, M E
PA (FURU-I) FURUKAWA T; (GAMB-I) GAMBINO J P; (KIEW-I) KIEWRA E W; (MAND-I) MANDELMAN J A; (RADE-I) RADENS C J; (TONT-I) TONTI W R; (WEYB-I) WEYBRIGHT M E; (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 2001014481 A1 20010816 (200154)* 31p
US 6380027 B2 20020430 (200235)
ADT US 2001014481 A1 US 1999-225127 19990104; US 6380027 B2 US 1999-225127 19990104
PRAI US 1999-225127 19990104
AB US2001014481 A UPAB: 20010924
NOVELTY - Array and support structures are made on a substrate simultaneously by forming a first oxide in a V-groove surface of the array structures and a second oxide on a planar surface of the support structures. The first oxide is thicker than the second oxide.
USE - The method is used for making array and support structures for semiconductor devices (claimed), e.g. metal oxide semiconductor field effect transistors (**MOSFETs**), **dynamic random**

access memories, read only memories, or electrically
programmable read only memories.
ADVANTAGE - The method can form relatively thin oxide layers for the support MOSFETs and simultaneously form thicker gate oxide layers for the array MOSFETs, thus increasing device performance and decreasing defects.
DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a semiconductor device.
Silicon structure 10
Thin thermal pad oxide layer 11
Silicon nitride pad layer 12
Oxide 13
Nitride 14
Stripes 15
Dwg.1/19

L27 ANSWER 7 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-235019 [29] WPIX
DNN N2002-180351 DNC C2002-071342
TI Method of manufacturing memory cell involves forming trench capacitor by etching filler material, substrate and **polysilicon** layer and replacing filler material with place holder material, at location corresponding to wordline gate conductor.
DC L03 U11
IN FURUKAWA, T; MANDELMAN, J A; TONTI, W R
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6271080 B1 20010807 (200229)* 41p
ADT US 6271080 B1 US 1999-465109 19991216
PRAI US 1999-465109 19991216
AB US 6271080 B UPAB: 20020508
NOVELTY - Memory cell fabrication method involves forming trench capacitor by etching filler material, substrate and **polysilicon** layer and then replacing filler material with place holder material, at location corresponding to wordline gate conductor.
DETAILED DESCRIPTION - A stack including a pad oxide layer, nitride pad layer, oxide layer and **polysilicon** layer is formed on a substrate. The stack is etched at preset locations and filled with filler material such as oxide. The trench capacitors are formed in the substrate by etching filler material, substrate and **polysilicon** layer. Then **polysilicon** layer and a portion of oxide layer are planarized. The portion of stack or filler material is replaced with place holder material at location corresponding to wordline gate conductor (42), for forming gate conductor.
USE - The method is used for fabricating memory cell such as 8F2 planar metal oxide semiconductor field effect transistor (**MOSFET**
) **dynamic random access memory**
(DRAM) cell.
ADVANTAGE - Eliminates wordline gate conductor to storage trench overlay sensitivity problem effectively.
DESCRIPTION OF DRAWING(S) - The figure shows fabrication process of 8F2 planar MOSFET DRAM cell.
Wordline gate conductor 42
Dwg.15/29

L27 ANSWER 8 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-214402 [27] WPIX
DNN N2002-164032 DNC C2002-065585
TI Formation of metal oxide semiconductor field effect transistor (MOSFET) for dynamic random access memory (DRAM) cell involves providing sacrificial layer to save portion of two **silicon** oxide layer during successive etching.

01/21/2003

DC L03 U11 U12 U13
IN HUANG, J; TSAI, C
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6265274 B1 20010724 (200227)* 12p
ADT US 6265274 B1 US 1999-431954 19991101
PRAI US 1999-431954 19991101
AB US 6265274 B UPAB: 20020429

NOVELTY - A metal oxide semiconductor field effect transistor is formed by providing two **silicon** oxide layers on gate and dielectric layer; providing sacrificial layer to save predetermined portion of the two **silicon** oxide layers; and performing successive etching to remove sacrificial layer on top of the gate, and the two **silicon** oxide layers on the protruding portion of the gate.

DETAILED DESCRIPTION - Formation of metal oxide semiconductor field effect transistor (MOSFET) on a wafer (30), comprising **silicon** substrate (12), and dielectric layer (14), involves forming a gate (16) on dielectric layer portion(s); forming a first **silicon** oxide layer (18) on the wafer, thus covering the gate; performing first ion implantation to form two doped areas (22) at two opposite sides of the gate used as lightly doped drains of the MOS transistor (38); forming a second **silicon** oxide layer (32) on the wafer, thus covering the first **silicon** oxide layer; forming sacrificial layer on the second **silicon** oxide layer; performing first etching to remove the sacrificial layer on top of the gate, causing the gate to protrude from the remaining sacrificial layer; performing a second etching process to remove the first and second **silicon** oxide layers on the protruding portion of the gate; removing the sacrificial layers; forming a **silicon** nitride layer on the wafer to cover the protruding portion of the gate and the remaining **silicon** oxide layers; performing a third anisotropic etching to remove the **silicon** nitride layer on top of the gate, thus forming a spacer (37); and performing a second ion implantation to form two doped areas on the substrate that are used as source and drain of the MOS transistor.

USE - Forming metal oxide semiconductor field effect transistor (MOSFET) used as pass transistor of dynamic random access memory cell (claimed).

ADVANTAGE - The method provides a substrate surface that is not coarsened by the ion implantation process, thus no short-circuiting occur between gate and the a subsequent contact plug.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a MOS transistor formed using the above process.

Substrate 12
Dielectric layer 14
Gate 16
Oxide layer 18, 32
Doped areas 22
Spacer 37
MOS transistor 38
Dwg.14/15

L27 ANSWER 9 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2001-285582 [30] WPIX
DNN N2001-203760 DNC C2001-087449
TI Semiconductor device manufacturing method e.g. metal oxide semiconductor transistor used in dynamic random access memory, involves forming side wall, by etching removal of **silicon** nitride film, deposited along inner wall of formed trench.
DC L03 U11 U13
IN KUNIKIYO, T
PA (MITQ) MITSUBISHI ELECTRIC CORP; (MITQ) MITSUBISHI DENKI KK

CYC 5
PI JP 2001036038 A 20010209 (200130)* 21p
CN 1282104 A 20010131 (200131)
DE 10022696 A1 20010531 (200131)
KR 2001020880 A 20010315 (200159)
US 2002151134 A1 20021017 (200270)
ADT JP 2001036038 A JP 1999-207522 19990722; CN 1282104 A CN 2000-108976 20000524; DE 10022696 A1 DE 2000-10022696 20000510; KR 2001020880 A KR 2000-27630 20000523; US 2002151134 A1 Div ex US 1999-476779 19991230, US 2002-121711 20020415
PRAI JP 1999-207522 19990722
AB JP2001036038 A UPAB: 20010603
NOVELTY - Insulating film (11) and **silicon** nitride film (12a, 12b) deposited on the side wall (10) of metal oxide semiconductor (MOS) transistor, are penetrated to the memory cell area (MA) to form trench. **Silicon** nitride film is deposited along the inner wall of trench and etching removal of nitride film is performed so that another side wall is formed on memory cell area adjacent to side wall (10).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device.
USE - The method is used for manufacturing semiconductor device such as MOS transistor used in dynamic random access memory (DRAM).
ADVANTAGE - Reduces leakage current without spoiling degree of integration by forming other side wall. The width of side wall of peripheral circuit formation area is comparatively narrow.
DESCRIPTION OF DRAWING(S) - The figure shows memory cell area of dynamic random access memory.
Side wall 10
Insulating film 11
Silicon nitride film 12a, 12b
Memory cell area MA
Dwg.1/35

L27 ANSWER 10 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2000-649218 [63] WPIX
CR 2001-171792 [60]
DNN N2000-481350 DNC C2000-196405
TI Tantalum nitride film formation method for capacitor used in dynamic random access memory, involves heating **silicon** substrate having tantalum oxide film to form titanium nitride film, in non-reactive gas atmosphere.
DC L03 U11 U12
IN YAMAMOTO, T
PA (NIDE) NEC CORP; (NIDE) NIPPON DENKI KK; (YAMA-I) YAMAMOTO T
CYC 2
PI JP 3045158 B1 20000529 (200063)* 6p
JP 2000160341 A 20000613 (200109) 6p
US 2002006739 A1 20020117 (200212)
ADT JP 3045158 B1 JP 1998-337542 19981127; JP 2000160341 A JP 1998-337542 19981127; US 2002006739 A1 US 1999-450351 19991129
PRAI JP 1998-337542 19981127; JP 1999-55185 19990303
AB JP 3045158 B UPAB: 20020221
NOVELTY - A **silicon** substrate (1) which has a tantalum oxide film (4) is heated at a temperature which lies between 400 deg. C or 700 deg. C. By heating under a non-reactive gas atmosphere and at the specified temperature, a titanium nitride film (5) is formed on the oxide film. Films (4,5) are capacitive film and plate electrode, respectively.
USE - For forming tantalum nitride film in capacitor used for metal oxide semiconductor field effect transistor (**MOSFET**), **dynamic random access memory** (DRAM).
ADVANTAGE - Since tantalum nitride film is formed on tantalum oxide

film in a non-reactive gas atmosphere, degradation in oxide film is prevented and therefore leakage of current is suppressed efficiently.
DESCRIPTION OF DRAWING(S) - The figures show sectional views of laminate structure during capacitor manufacture.
Silicon substrate 1
Tantalum-oxide film 4
Titanium nitride film 5
Dwg.1/6

L27 ANSWER 11 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1999-435775 [37] WPIX
DNN N1999-325095 DNC C1999-128321
TI **Silicon** oxide film formation for MOS-type semiconductor device, e.g. MOSFET and dynamic random access memory - involves forming protection oxide film on **silicon** substrate having flat surface on nuclear level.
DC L03 U11 U12
PA (FUIT) FUJITSU LTD; (HITA) HITACHI LTD; (NIDE) NEC CORP
CYC 1
PI JP 11176828 A 19990702 (199937)* 9p
ADT JP 11176828 A JP 1997-342476 19971212
PRAI JP 1997-342476 19971212
AB JP 11176828 A UPAB: 19990914
NOVELTY - A **silicon** oxide film (4) is formed on surface of **silicon** substrate (1) by heat oxidation, and the temperature of the substrate is maintained between 500-700 deg. C. A protection oxide film (3) is formed on the surface of the **silicon** substrate having a flat surface (2) on nuclear level.
USE - In MOS-type semiconductor device, e.g. DRAM, MOSFET.
ADVANTAGE - Enables miniaturization of MOSFET by making the boundary surface of the gate oxide film flat at a nuclear level. Reduces roughness of boundary surface of the **silicon** oxide film. Improves reliability of semiconductor device with high integration degree.
DESCRIPTION OF DRAWING - The figure explains the method involved during formation of **silicon** oxide film. (1) **Silicon** substrate; (2) Flat surface; (3) Protection oxide film; (4) **Silicon** oxide film.
Dwg.1/7

L27 ANSWER 12 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1998-176299 [16] WPIX
DNN N1999-088676 DNC C1999-035681
TI MOSFET for use with DRAM - has N type impurities ion implanted in a P type substrate, forming a well, and a buried channel formed with P type impurities implanted at a lower energy.
DC L03 U11 U12 U13 U14
IN NOH, K; NOH, G M; RHO, K M
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD
CYC 3
PI KR 97013412 A 19970329 (199816)*
US 5861334 A 19990119 (199911)B 9p
TW 371367 A 19991001 (200036)
KR 172793 B1 19990201 (200039)
ADT KR 97013412 A KR 1995-24299 19950807; US 5861334 A US 1996-692622 19960806; TW 371367 A TW 1996-109430 19960805; KR 172793 B1 KR 1995-24299 19950807
PRAI KR 1995-24299 19950807
AB US 5861334 A UPAB: 19990316 ABEQ treated as Basic
Semiconductor device is made by forming a field oxide film (13) on a P type substrate (11) by local oxidation of **silicon** (LOCOS). An N type profiled well (14) is formed in the substrate by high energy ion

implantation. Further N type impurities are implanted in the top of the well (15), compensating for the N type impurity density in a buried channel (16), which is formed by implantation of P type impurities at a lower energy. A gate oxide film (17) and a gate electrode (18) are formed on the substrate surface.

The P-type impurities are formed using BF2 as a source, at a dose of 8x1012 and a maximum energy of 20 keV, whereas the N type uses phosphorous as a source, at a dose of 3x1012 and a maximum energy of 40 keV.

ADVANTAGE - Short channel and on/off characteristics are improved by enhancing the N type ion density at the region beneath the buried channel.
Dwg.7/10

L27 ANSWER 13 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1992-132354 [16] WPIX
DNN N1992-098716
TI Highly integrable **MOS dynamic random-access memory** - has elongated trenches at right angles to line joining source and drain regions under gate dielectric.
DC U11 U12 U13
IN STEIN, K U
PA (SIEI) SIEMENS AG
CYC 15
PI WO 9205584 A 19920402 (199216)* DE 15p
RW: AT BE CH DE DK ES FR GB GR IT LU NL SE
W: JP US
ADT WO 9205584 A WO 1991-DE519 19910626
PRAI DE 1990-4029108 19900913
AB WO 9205584 A UPAB: 19931006
In the surface of an e.g. monocrystalline Si substrate (11), active circuit elements are separated by field oxide regions (12) surrounding a MOSFET with a number of 0.1-micron wide trenches (14) between source and drain regions (13). These regions are covered and the trenches (14) lined with 20 nm thick gate dielectric (15a) to which a doped **polysilicon** gate electrode (16) is applied.

The trenches (14) may be formed e.g. by electron beam lithography or by a laser interference method giving finer structure.

ADVANTAGE - Less substrate area is occupied without detriment to power-handling capacity of MOSFET. (1/4)
1/4

L27 ANSWER 14 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:14249 HCAPLUS
DN 116:14249
TI Semiconductor devices
IN Tomita, Yutaka
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03191567	A2	19910821	JP 1989-332062	19891220

PRAI JP 1989-332062 19891220
AB The title device useful for an **MOS dynamic random-access memory** device comprises (1) a groove formed on a 1st cond.-type substrate, (2) an insulator film for an interlayer insulation region formed on the internal surface of the groove, (3) a 1st elec. conductive layer for a capacitor contact formed on the insulator film, (4) a 1st dielec. layer formed on the 1st elec. conductive

layer, (5) a 2nd elec. conductive layer for a const.-voltage capacitor contact formed on the 1st dielec. layer, (6) a 2nd dielec. layer formed on the 2nd elec. conductive layer, and (7) a 3rd elec. conductive layer for a capacitor contact formed on the 2nd dielec. layer. The use of the internal surface of the groove as a sepg. insulator for memory cells had addnl. 2 capacitors equiv to 2 bids in the groove to save the surface area of the memory cell.

L27 ANSWER 15 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1989-010560 [02] WPIX
TI **MOS dynamic random-access memory** - has bit-line contact hole on **poly silicon** formed on transistor drain and source layers. NoAbstract Dwg 1/14.
DC U12 U13 U14
PA (HITA) HITACHI LTD
CYC 1
PI JP 63281457 A 19881117 (198902)*
ADT JP 63281457 A JP 1987-114630 19870513
PRAI JP 1987-114630 19870513

L27 ANSWER 16 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1987-192327 [27] WPIX
DNN N1987-143991
TI Semiconductor dynamic RAM memory array - has bit lines organised into pairs of adjacent **poly silicon** lines coupled to memory cells in alternating configuration.
DC U14
IN KARP, J A
PA (VISI-N) VISIC INC
CYC 1
PI US 4675848 A 19870623 (198727)* 10p
ADT US 4675848 A US 1984-621848 19840618
PRAI US 1984-621848 19840618
AB US 4675848 A UPAB: 19930922
The **MOS dynamic random access memory** (DRAM) device has an array of dynamic RAM cells accessed by word and bit lines. Each memory cell comprises a single field-effect transistor coupled by its source to the gate of an MOS storage capacitor. The word lines are coupled to their respective memory cells at the gate of the field-effect transistor, while the bit lines are coupled to their respective memory cells at the drain of the field-effect transistor.
The bit lines are organised into pairs of adjacent **polysilicon** lines that are coupled to all the memory cells on both sides of the bit lines in an alternating configuration. The word lines are coupled to alternating pairs of cells on opposite sides of the word lines.
ADVANTAGE - Allows 265K memory to fit into 16-pin plastic package.
3/14

L27 ANSWER 17 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 1985:141885 HCAPLUS
DN 102:141885
TI MOS dynamic memory cells
IN Ogura, Mitsugi
PA Toshiba Corp., Japan
SO U.S., 11 pp. Cont. of U.S. Ser. No. 104,866, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

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PI   US 4492973       A    19850108        US 1981-335601  19811230
PRAI JP 1978-158709        19781225
     JP 1978-158710        19781225
     US 1979-104866        19791218
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AB The memory cell described can be written with voltage nearly equal to the power supply voltage, thereby increasing by .apprx.33% the charge stored in the MOS capacitor. Thus, the operation range of the sense circuit can be broadened. Reliability and manufg. yield of the memory cells also can be improved. The MOS dynamic memory cell comprises a 1st elec. conductive layer formed on a surface of a 1st region of a semiconductor substrate having a 1st cond. type and an impurity concn. of <5 .times. 1014 cm-3 through a 1st insulating film, a 2nd semiconductor region having a higher impurity concn. than the 1st semiconductor region and provided adjacent to 1 end of the 1st semiconductor region, a 2nd elec. conductive layer formed on the 2nd semiconductor region through a 2nd insulating film, and a 3rd semiconductor region of a 2nd cond. type and provided adjacent to the 2nd semiconductor region. The 2nd elec. conductive layer is used as a row line, whereas the 3rd semiconductor region is used as a column line as well as a digit line. An inversion layer is formed on a surface of the 1st semiconductor region. The MOS dynamic memory cell is used to fabricate a **MOS dynamic random access memory**. The 1st and 2nd elec. conductive layers may be made of Mo or Mo silicide. Alternatively, they may be made of polycryst. Si and used with insulating films of SiO2.

L27 ANSWER 18 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 1983:462455 HCAPLUS
DN 99:62455
TI Some observations on oxygen precipitation/gettering in device processed Czochralski **silicon**
AU Huff, H. R.; Schaake, H. F.; Robinson, J. T.; Baber, S. C.; Wong, D.
CS Texas Instrum., Inc., Dallas, TX, 75265, USA
SO Journal of the Electrochemical Society (1983), 130(7), 1551-5
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
AB The thermal history and O and C concns. control the Si material properties and much of the subsequent circuit performance. The beneficial effect of intrinsic gettering due to pptn. of O in the bulk on MOS dynamic RAM refresh performance is shown. Equivalent thermal processes result in similar circuit performance only when the Si material is equiv. Some circumstantial evidence is also presented for a degrading effect of high concns. of C in the starting material.

L27 ANSWER 19 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 1982:573270 HCAPLUS
DN 97:173270
TI The effect of substrate materials on holding time degradation in MOS dynamic RAM
AU Otsuka, H.; Watanabe, K.; Nishimura, H.; Iwai, H.; Nihira, H.
CS Integr. Circuit Div., Toshiba Corp., Kawasaki, 210, Japan
SO IEEE Electron Device Letters (1982), EDL-3(7), 182-4
CODEN: EDLEDZ; ISSN: 0193-8576
DT Journal
LA English
AB The effect of substrate materials (bulk Si, p/p+ epitaxial Si and intrinsic gettering Si) on the holding-time degrdn. of **MOS dynamic** RAM (**random-access memory**) cells by excess minority carriers emitted from adjacent MOS devices was studied. Intrinsic gettering Si has less susceptibility to holding-time

degrdn. than p/p+ epitaxial Si and much less than bulk Si. The degrdn. mechanism is discussed in connection with the substrate materials.

L27 ANSWER 20 OF 24 JAPIO COPYRIGHT 2003 JPO
AN 1981-067960 JAPIO
TI **MOS DYNAMIC RANDOM ACCESS MEMORY**
IN FUJISHIMA KAZUYASU
PA MITSUBISHI ELECTRIC CORP
PI JP 56067960 A 19810608 Showa
AI JP 1979-143478 (JP54143478 Showa) 19791105
PRAI JP 1979-143478 19791105
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1981
AB PURPOSE: To prevent a noise during selecting a word line by a method wherein a transfer transistor in capacity coupling with a gate composing a capacitor of an MOS dynamic RAM and earthed to the ground through a resistor is installed.
CONSTITUTION: A memory cell is earthed to the ground through a resistor 10 or a transistor and is composed of an N<SP>+</SP> diffusion layer 1 constituting a bit line, the 1st layer **polysilicon** gate 9 connected to a word storage line, a resistor 10 or a transistor, a grounded word line 8 of the 2nd layer **polysilicon** gate constituting a transfer transistor, a gate oxide film 4 and a field oxide film 5. The word storage line and the grounded word line are in a capacity coupling. And during selection of a word storage line, the grounded line deflects to a negative side owing to its capacity coupling, however, a noise is not induced at a bit line, thus, enabling a preparation of a large capacity memory.
COPYRIGHT: (C)1981,JPO&Japio

L27 ANSWER 21 OF 24 JAPIO COPYRIGHT 2003 JPO
AN 1981-067959 JAPIO
TI **MOS DYNAMIC RANDOM ACCESS MEMORY**
IN FUJISHIMA KAZUYASU
PA MITSUBISHI ELECTRIC CORP
PI JP 56067959 A 19810608 Showa
AI JP 1979-143476 (JP54143476 Showa) 19791105
PRAI JP 1979-143476 19791105
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1981
AB PURPOSE: To prevent unequality of a cell capacitance by a method wherein a separating gate is used to separate a word line of an MOS dynamic RAM from a memory cell and an MOS capacitance is constituted with the 2nd layer **polysilicon** gate.
CONSTITUTION: An 1-transistor 1-capacitor type memory cell consists of an N<SP>+</SP> diffusion area 11 constituting a bit line, the 1st layer **polysilicon** gate 12 constituting a word line, a separating gate 16 wherein a VSS voltage is applied to separate each memory cell one another, the 2nd layer **polysilicon** gate 13 constituting an MOS capacitor and a gate oxide film 14. And during the 1st layer **polysilicon** gate being formed, each of the gate are of a transfer transistor, the area of an MOS capacitor and the area of an N<SP>+</SP> diffusion layer is decided and they are equal without depending upon an error of a mask matching, thus, resulting in each equal cell capacitance and each equal bit line capacitance.
COPYRIGHT: (C)1981,JPO&Japio

L27 ANSWER 22 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 1981:613924 HCAPLUS
DN 95:213924
TI Reliability evaluation of aluminum-metallized MOS dynamic rams in plastic

packages in high humidity and temperature environments
AU Striny, Kurt M.; Schelling, Arthur W.
CS Bell Lab., Allentown, PA, 18103, USA
SO Proceedings - Electronic Components Conference (1981), 31st, 238-44
CODEN: PECCA7; ISSN: 0569-5503
DT Journal
LA English
AB Acceleration factors detd. by anal. using an Eyring model (Gladstone, S.; Laidler, K. L., 1941) and parameters detd. from published Al corrosion data and applied to stress test results showed that Al-metalized n-channel **MOS dynamic random-access memories** (RAM's) in plastic packages are reliable under typical use environments. The use of Si3N4 passivation, room-temp.-vulcanizable silicone rubber encapsulation, and effective cleaning are probably the leading factors in achieving the improved performance over that obsd. on com. devices in plastic packages. Devices operating with some power dissipation experience significantly lower failure rates. Confidence of this anal. is obtained by using conservative assumptions throughout and using worst-case use conditions to est. the failure rate expected after 40 yr in the field.

L27 ANSWER 23 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 1980:207820 HCAPLUS
DN 92:207820
TI Semiconductor device with double layer gate structure
IN Iwai, Hiroshi
PA Cho LSI Gijutsu Kenkyu Kumiai, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 55003649	A2	19800111	JP 1978-75609	19780622
PRAI	JP 1978-75609		19780622		

AB A method is claimed for fabricating semiconductor devices (e.g. **MOS dynamic random-access memory**) having a double-layer gate electrode (e.g. polycryst. Si, P-doped polycryst. Si, Mo silicide, etc.) structure.

L27 ANSWER 24 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 1978:181179 HCAPLUS
DN 88:181179
TI Development of the N-channel **silicon** gate 1024 bit MOS RAM
CS Peking University, "1024" Dev. Group, Fact. Electron. Instrum., Peking, Peop. Rep. China
SO Beijing Daxue Xuebao, Ziran Kexueban (1977), (1), 13-31
CODEN: PCTHAP; ISSN: 0479-8023
DT Journal
LA Chinese
AB The prodn. of a N-channel Si gate MOS random access memory is described. The surface defects of the Si element were treated with MgO or Cu or Cr ion polishing. The optimum HCl/O2 ratio for surface treatment and oxidn. is 8-10%, which yields a current carrier d. of 1010 cm-2. The etching procedure and the evapn. of Al contacts are described. The BD 7503 N-channel Si gate 1024 bit **MOS dynamic random access memory** has an access time of 80 ns and a cycle time of 200 ns. at an operating power of <150 mv.

L29 ANSWER 1 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 2002-132687 [18] WPIX
CR 1987-023150 [04]; 1989-063571 [09]; 1990-047952 [07]; 1991-180044 [25]; 1992-064482 [08]; 1993-117076 [14]; 1995-043719 [06]; 1995-114943 [15]; 1998-236272 [21]; 1998-236274 [21]; 1998-568044 [48]; 2000-202326 [18]; 2000-202327 [18]; 2001-089792 [56]
DNN N2002-100096
TI Semiconductor device e.g. dynamic random access memory, has control circuit which impresses control voltage to transistor through which internal voltage is supplied to source node of CMOS circuit.
DC U13 U14 U21
PA (HITA) HITACHI LTD
CYC 1
PI JP 2001036021 A 20010209 (200218)* 30p
JP 3216642 B2 20011009 (200218) 29p
ADT JP 2001036021 A Div ex JP 1999-197006 19880506, JP 2000-157953 19880506; JP 3216642 B2 Div ex JP 1999-197006 19880506, JP 2000-157953 19880506
FDT JP 3216642 B2 Previous Publ. JP 2001036021
PRAI JP 1999-197006 19880506; JP 2000-157953 19880506
AB JP2001036021 A UPAB: 20020319
NOVELTY - The semiconductor device has voltage converting circuit (3A) which converts external voltage (Vcc) to corresponding internal voltage. An internal circuit (2) which contains a CMOS circuit (DRIV) is provided to supply the internal voltage to source node of CMOS circuit through a MOS transistor (ICL). Control circuit (3B) impresses a control voltage (VCONT) to gate of MOS transistor.

USE - Semiconductor devices such as metal oxide semiconductor (**MOS) dynamic random access memory** (DRAM), synchronous random access memory (SRAM).

ADVANTAGE - The stability and reliability of high integration semiconductor device are improved at a low cost.

DESCRIPTION OF DRAWING(S) - The figure shows circuit diagram of semiconductor device.

Internal circuit 2
Voltage converting circuit 3A
Control circuit 3B
Dwg.16/70

L29 ANSWER 2 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 2000-170676 [15] WPIX
CR 1996-353928 [35]; 1999-106856 [10]
DNN N2000-126899
TI Shallow trench isolation structure formation method for MOSFET in dynamic random access memory cell.
DC U11 U12 U13 U14
IN EL-KAREH, B; GHATALIA, A K; NOBLE, W P
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6022781 A 20000208 (200015)* 10p
ADT US 6022781 A Div ex US 1994-365729 19941228, US 1996-772708 19961223
FDT US 6022781 A Div ex US 5539229
PRAI US 1994-365729 19941228; US 1996-772708 19961223
AB US 6022781 A UPAB: 20000323
NOVELTY - Insulator (48) is deposited in a trench which is formed by removing a portion of gate stand. The insulator is planarized to provide a raised trench isolation. The remaining portions of gate stack are removed to provide a segment gate. The trench insulator is self aligned with the edges of segment gate. A wiring level which comprises a conductive spacer, is deposited such that it contacts the segment gate.

USE - For a metal-oxide-semiconductor field-effect transistor

(MOSFET) in a dynamic random access memory (DRAM) cell.
ADVANTAGE - Avoids thinning of gate dielectric adjacent to the trench corner. Avoids corner leakage without degrading device performance.
DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of the shallow trench isolation structure.
Insulator 48
Dwg.8/13

L29 ANSWER 3 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1993-062747 [08] WPIX
CR 2002-295583 [72]
DNN N1994-119066
TI High density integrated circuit semiconductor memory e.g. DRAM - has bit line level potential set at higher value than that of non-selective word line, thus increases time of current disconnection by using lower threshold voltage of memory cell transfer gate MOS transistor.
DC U13 U14
IN KATO, D; OOWAKI, Y; TAKASHIMA, D
PA (TOKE) TOSHIBA KK; (TOKE) TOSHIBA CORP
CYC 3
PI JP 05012866 A 19930122 (199308)* 32p
US 5299154 A 19940329 (199419)B 44p
US 5426604 A 19950620 (199530) 43p
US 5638329 A 19970610 (199729) 42p
KR 9509228 B1 19950818 (199843)
US 5870339 A 19990209 (199913)
US 5969998 A 19991019 (199950)
ADT JP 05012866 A JP 1991-161899 19910702; US 5299154 A US 1992-907645 19920702; US 5426604 A Cont of US 1992-907645 19920702, US 1994-197409 19940216; US 5638329 A Cont of US 1992-907645 19920702, Cont of US 1994-197409 19940216, US 1995-420079 19950411; KR 9509228 B1 KR 1992-11813 19920702; US 5870339 A Cont of US 1992-907645 19920702, Cont of US 1994-197409 19940216, Cont of US 1995-420079 19950411, US 1996-742924 19961101; US 5969998 A Cont of US 1992-907645 19920702, Cont of US 1994-197409 19940216, Cont of US 1995-420079 19950411, Cont of US 1996-742924 19961101, US 1998-213773 19981217
FDT US 5426604 A Cont of US 5299154; US 5638329 A Cont of US 5299154, Cont of US 5426604; US 5870339 A Cont of US 5299154, Cont of US 5426604, Cont of US 5638329; US 5969998 A Cont of US 5299154, Cont of US 5426604, Cont of US 5638329, Cont of US 5870339
PRAI JP 1991-161899 19910702
AB US 5299154 A UPAB: 19940627 ABEQ treated as Basic
The MOS DRAM includes multiple of pairs of bit lines, and word lines transverse to the bit lines to define cross-points, at which an array of memory cells are arranged. Each cell has storage capacitor and a transfer gate MOS transistor having a gate coupled to a word line and being connected between the capacitor and a bit line.
Sense amplifiers are connected to the bit line pairs, and have a first and second common source line. A decoder and a word line driver are connected to the word lines. A MOS transistor is connected between the power voltage and the first common source line, for selectively supplying it with a first voltage, which potentially defines a high level voltage for the bit line pairs.
USE/ADVANTAGE - As high integrated DRAM contg capacitive elements and data transfer transistor. Improved performance and better reliability.
Dwg.7/47
AB JP 05012866 A UPAB: 20020528
Dwg.1/55

L29 ANSWER 4 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1990-158056 [21] WPIX

01/21/2003

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DNN  N1990-122831
TI   Video display system with cellular bit-mapped memory - is coupled to
     microprocessor by control bus which supplies basic clock frequency for
     serial video data output.
DC   P85 T01 T04
IN   HUGHES, J M; LAFTITTE, D S; MCDONOUGH, K C
PA   (TEXI) TEXAS INSTR INC
CYC  4
PI   EP 369994     A  19900523 (199021)*
         R: DE FR GB NL
ADT  EP 369994 A EP 1983-100604 19830914
PRAI US 1982-427256    19820929
AB   EP    369994 A UPAB: 19930928
     Video signals are supplied to a raster-scan CRT with horizontal and
     vertical scanning and sync circuits and signal shaping circuits from a
     bit-mapped video memory. The memory has an additional parallel port
     coupled to the multiplexed address-data input output bus of a
     microprocessor. Rows and columns of memory cells in an array are
     partitioned according to the size and type of video display. Different
     clock signals are supplied for operation of the microprocessor and for
     shifting video data out of a register.
          USE/ADVANTAGE - With microcomputer-based word processors or
     interactive TV. Mass-producible MOS dynamic
     random-access memory combines additional
     sequential serial access capability for high-resoln. colour video displays
     wiht traditional parallel access capability without loss of performance.
     4/8

L29  ANSWER 5 OF 35  WPIX (C) 2003 THOMSON DERWENT
AN   1990-158055 [21]    WPIX
CR   1984-115650 [19];  1990-173292 [23];  1990-187471 [25]
DNN  N1990-122830
TI   Video display system with cellular bit-mapped memory - accessed via serial
     input register port and bit-parallel input port for parallel read out and
     writing.
DC   P85 T01 T04
IN   HUGHES, J M; LAFFITTE, D S; MCDONOUGH, K C
PA   (TEXI) TEXAS INSTR INC
CYC  4
PI   EP 369993     A  19900523 (199021)*
         R: DE FR GB NL
ADT  EP 369993 A EP 1983-100603 19830914
PRAI US 1982-427236    19820929
AB   EP    369993 A UPAB: 19950530
     Video signals (2) are supplied to a raster-scan CRT (1) with horizontal
     and vertical scanning and sync circuits (3) and signal shaping circuits
     (4), from a bit-mapped video memory (5). The memory has an additional
     parallel port (6) coupled to the multiplexed address/data input/output bus
     (7) of a microprocessor (8).
          Rows and columns of memory cells in an array (10) are partitioned
     according to the size and type of video display. For serial input/output a
     256-bit shift register (20) is divided into halves on opposite sides of
     the array.
          USE/ADVANTAGE - With microcomputer-based word processors or
     interactive TV. Mass-producible MOS dynamic
     random-access memory combines additional
     sequential serial access capability for high-resoln. volour video displays
     with traditional parallel access capability, without loss of performance.
     @(20pp Dwg.No.1/8)@
     1/8
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01/21/2003

L29 ANSWER 6 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1989-352731 [48] WPIX
TI Semiconductor device of **MOS dynamic random access memory** - uses layer of losing entrap of unwanted impurity to form capacity around electrode of accumulating capacitor NoAbstract Dwg 1/3.
DC U11 U12 U13
PA (AGEN) AGENCY OF IND SCI & TECHNOLOGY
CYC 1
PI JP 01264256 A 19891020 (198948)*
ADT JP 01264256 A JP 1988-91702 19880415
PRAI JP 1988-91702 19880415

L29 ANSWER 7 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1988-128728 [19] WPIX
TI DRAM device mfr. for reducing cell size - by forming connecting hole between capacitor and MISFET in side wall of capacitor trench NoAbstract Dwg 8/8.
DC L03 U12 U13 U14
PA (HITA) HITACHI LTD
CYC 1
PI JP 63070559 A 19880330 (198819)* 3p
ADT JP 63070559 A JP 1986-213861 19860912
PRAI JP 1986-213861 19860912

L29 ANSWER 8 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1988-108641 [16] WPIX
TI Semiconductor memory circuit device mfr. - with vol. element and MOSFET and has structure of fine memory element, optimum to **MOS dynamic random access memory**
NoAbstract Dwg 1a-e/5.
DC L03 U11 U13 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 63056954 A 19880311 (198816)* 4p
ADT JP 63056954 A JP 1986-203006 19860828
PRAI JP 1986-203006 19860828

L29 ANSWER 9 OF 35 JAPIO COPYRIGHT 2003 JPO
AN 1988-299261 JAPIO
TI MANUFACTURE OF **MOS DYNAMIC RANDOM ACCESS MEMORY**
IN KIYONO JUNJI
PA NEC CORP
PI JP 63299261 A 19881206 Showa
AI JP 1987-134571 (JP62134571 Showa) 19870529
PRAI JP 1987-134571 19870529
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To form an impurity distribution having a desired profile at sidewalls of a groove with high accuracy by a method wherein, when an impurity is to be introduced into the sidewalls of the groove, ions are implanted while a semiconductor substrate where the groove capacitance is formed is tilted with reference to an ion beam and is turned.
CONSTITUTION: Ions of boron are implanted by making use of a resist mask 5 as a mask. As a condition for ion implantation, a semiconductor substrate 1 is tilted by 10° with reference to an ion beam and this semiconductor substrate 1 is turned mechanically at a speed of one revolution per second; first P-type impurity regions 9, 10 are thus formed. Furthermore, an angle of the semiconductor substrate with reference to the ion beam is changed to 30°; the ions are implanted in the same manner while the substrate is turned; second P-type impurity

regions 11, 12 are thus formed. The first P-type impurity regions are not implanted near the surface at the sidewalls of the groove due to a shadow by protruding parts 8 at the resist mask 5; the second P-type impurity regions where the ions are implanted with a tilt of a bigger angle are formed in these regions.

L29 ANSWER 10 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1987-174632 [25] WPIX
TI **MOS dynamic random-access memory** device - has gate insulation film on impurity-doped diffusion layer NoAbstract Dwg 2/3.
DC U12 U13 U14
PA (MATE) MATSUSHITA ELECTRONICS CORP
CYC 1
PI JP 62106658 A 19870518 (198725)* 5p
ADT JP 62106658 A JP 1985-247453 19851105
PRAI JP 1985-247453 19851105

L29 ANSWER 11 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1987-165517 [24] WPIX
DNN N1987-124094
TI Metal-oxide-semiconductor dynamic RAM - has sense amplifier coupled to bit line pair and includes pair of imbalanced capacitors coupled to receive signal during sensing.
DC U14
IN KUNG, R I; SCHUTZ, J D
PA (ITLC) INTEL CORP
CYC 1
PI GB 2184311 A 19870617 (198724)*
GB 2184311 B 19880525 (198821)
ADT GB 2184311 A GB 1987-441 19820426
PRAI US 1984-582526 19840222
AB GB 2184311 A UPAB: 19930922
The dynamic RAM has its bit line pairs precharged to half the supply voltage by shorting the lines together at the start of an active cycle, one of the lines having previously been restored to a full supply potential, the other to ground potential, no separate reference potential being used. This ensures that a mid-supply reference voltage is used which reflects the actual supply voltage immediately prior to the access operation. asymmetrical capacitor pairs (kick control) compensate for parasitic couplings.

Active RESTORE circuits ensure full logic levels are stored in cells and read out as data. A sense amplifier is coupled to pair of bit lines and includes two pairs of imbalanced capacitors coupled to the sense amplifier and coupled to receive a signal during sensing. Thus only one of the set of capacitors receive the signal during sensing to provide compensation for parasitic coupling to the bit lines.
2/6

L29 ANSWER 12 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1987-165516 [24] WPIX
DNN N1987-124093
TI Metal-oxide-semiconductor dynamic RAM - has restore circuit causing one bit line to be at full supply potential and other to be at ground potential prior to sensing.
DC U14
IN KUNG, R I; SCHUTZ, J D
PA (ITLC) INTEL CORP
CYC 1
PI GB 2184310 A 19870617 (198724)*

```
     GB 2184310    B  19880525 (198821)
ADT  GB 2184310 A GB 1987-440 19820426
PRAI US 1984-582526    19840222
AB   GB   2184310 A UPAB: 19930922
```

The MOS DRAM includes a sense amplifier and a pair of bit lines. The sense amplifier includes unbalanced pairs of capacitors connected to the bit lines. One of the other capacitor pairs is energised immediately prior to a SENSE operation according to whether the selected cell is connected to the upper or lower bit line. This compensates for parasitic coupling and ensures that a true reference voltage midway between the supply voltage and ground is obtained.

Prior to sensing, a RESTORE circuit ensures that one bit line is at the full supply potential and the other is at ground potential. The bit lines are then shorted together to provide the basic mid-level reference potential, no dummy cells being required.

2/6

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L29  ANSWER 13 OF 35  WPIX (C) 2003 THOMSON DERWENT
AN   1987-165515 [24]   WPIX
DNN  N1987-124092
```

TI Metal-oxide-semiconductor dynamic RAM - has restorer coupled to each pair of bit lines to ensure ground potential at one pair and supply potential at other.

```
DC   U14
IN   KUNG, R I; SCHUTZ, J D
PA   (ITLC) INTEL CORP
CYC  1
PI   GB 2184309    A  19870617 (198724)*
     GB 2184309    B  19880525 (198821)
ADT  GB 2184309 A GB 1987-439 19820426
PRAI US 1984-582526    19840222
AB   GB   2184309 A UPAB: 19930922
```

The memory comprises a first and second pairs of bit lines, a number of memory cells coupled to the bit lines and a sense amplifier. A multiplexer selectively couples one of the first and second pairs of bit lines to the sense amplifier and is coupled to the first and second pairs of bit lines and the sense amplifier. Two restorers are included for restoring potentials on the first and second pairs of bit lines, respectively, and are coupled to the pairs of bit lines. The two restorers are separately activated from restoring potentials on the two pairs of bit lines, whereby current peaks for the DRAM are reduced.

The sense amplifier is fabricated from devices of a first conductively type and the restorers are fabricated from transistors of a second conductivity type.

2/6

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L29  ANSWER 14 OF 35  HCAPLUS  COPYRIGHT 2003 ACS
AN   1986:506858  HCAPLUS
DN   105:106858
TI   Semiconductor device
IN   Ito, Yasuo; Ogura, Isao; Numata, Kenji
PA   Toshiba Corp., Japan
SO   Jpn. Kokai Tokkyo Koho, 5 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1
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	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61082435	A2	19860426	JP 1984-204417	19840929
PRAI	JP 1984-204417		19840929		

AB A method for fabricating a semiconductor device (e.g., **MOS dynamic random-access memory** device)
involves the following steps: (1) forming an electrode-material film (e.g., polycryst. Si) on a semiconductor substrate via an insulator film; (2) covering the electrode-material film with a mask having a predetd. pattern; and (3) carrying out anisotropic and then isotropic etching of the electrode-material film to prep. an electrode without an overhung structure.

L29 ANSWER 15 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1987-011946 [02] WPIX
TI **MOS dynamic random access memory** - has low-impedance mesh electrode layer buried in memory cell isolation region NoAbstract Dwg 3/4.
DC U13 U14
PA (MITQ) MITSUBISHI DENKI KK
CYC 1
PI JP 61270863 A 19861201 (198702)* 5p
ADT JP 61270863 A JP 1985-112857 19850525
PRAI JP 1985-112857 19850525

L29 ANSWER 16 OF 35 WPIX (C) 2003 THOMSON DERWENT DUPLICATE 1
AN 1985-232949 [38] WPIX
TI **MOS dynamic random access memory** device - has opposite direction voltage applied between N-type semiconductor board and p-type semiconductor layer formed on it NoAbstract Dwg 2/2.
DC U13 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 60150664 A 19850808 (198538)* 18p
ADT JP 60150664 A JP 1984-6609 19840118
PRAI JP 1984-6609 19840118

L29 ANSWER 17 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1985-225348 [37] WPIX
DNN N1985-169283
TI CMOS D-RAM with multiplexed bit lines to sense amplifiers - has restore circuits separately activated for each pair of bit lines, and which are deactivated during writing.
DC U14
IN KUNG, R I; SCHUTZ, J D
PA (ITLC) INTEL CORP
CYC 2
PI GB 2154821 A 19850911 (198537)* 11p
US 4584672 A 19860422 (198619)
GB 2154821 B 19880525 (198821)
ADT GB 2154821 A GB 1985-2632 19850201; US 4584672 A US 1984-582526 19840222
PRAI US 1984-582526 19840222
AB GB 2154821 A UPAB: 19930925
Two pairs of bit lines (25,26, and 23,24) are selectively coupled to a single sense amplifier (30) by multiplexing. Both pairs of bit lines are decoupled from the sense amplifier (by 32,33) after a word line selects a cell and before sensing occurs in the sense amplifier. Only one pair of bit lines is coupled to the input/output lines of the memory. No dummy cells are employed. The bit lines are charged to one-half the power supply potential by first charging one bit line to the power supply voltage and the other to ground, and then shorting the bit lines together.

Restoration of potentials on each pair of bit lines occurs at different times, thereby reducing the peak currents to the RAM. Precharge takes place during the active memory cycle. A boost signal (kick capacitor

control) couples to one or the other pairs of bit lines via capacitors which have different values so as to compensate for asymmetry during sensing.
ADVANTAGE - Less power consumed and reduces peak currents.
4/4

L29 ANSWER 18 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1985-311723 [50] WPIX
DNN N1985-231436
TI Integrated circuit protection with integrated voltage converter - generates internal voltage higher than supply voltage only after supply transient ceases.
DC U13 U14 U24
IN HORI, R; ITOH, K
PA (HITA) HITACHI LTD
CYC 5

PI	DE 3519249	A	19851205	(198550)*	60p
	GB 2161664	A	19860115	(198603)	
	US 4691304	A	19870901	(198737)	
	GB 2161664	B	19881102	(198844)	
	JP 04263194	A	19920918	(199244)	13p
	DE 3519249	C2	19930318	(199311)	14p
	KR 9305977	B1	19930630	(199425)	
	KR 9403891	B1	19940504	(199607)	
	KR 9403892	B1	19940504	(199607)	

ADT GB 2161664 A GB 1985-13412 19850528; US 4691304 A US 1985-739092 19850530; JP 04263194 A Div ex JP 1984-108365 19840530, JP 1991-124349 19840530; DE 3519249 C2 DE 1985-3519249 19850529; KR 9305977 B1 Div ex KR 1985-3473 19850521, KR 1993-1655 19930208; KR 9403891 B1 KR 1985-3473 19850521; KR 9403892 B1 Div ex KR 1985-3473 19850521, KR 1993-13390 19930716
PRAI JP 1984-108365 19840530
AB DE 3519249 A UPAB: 19930925
At least one voltage converter (400) transforms an external voltage supply (VCC) into another internal voltage (VINT) in the chip. At least a part of the circuits in the chip use the internal voltage (VINT) as a reference voltage.
The internal voltage (VINT) is so controlled that, by switching on the external voltage supply (100), the internal voltage (VINT) begins to rise later or for the rise to need a longer time span than the external supply voltage (VCC).
USE/ADVANTAGE - Semi-conductor units, e.g. **MOS dynamic random access memory** (DRAM).
Current spikes which might damage the appts. supplying the power to the unit are eliminated. The problem of voltage fluctuations due to faulty operation during normal operation of the supply source, causing current spikes, is solved.
13A/20

L29 ANSWER 19 OF 35 JAPIO COPYRIGHT 2003 JPO
AN 1984-114863 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN HASEGAWA HITOSHI
PA FUJITSU LTD
PI JP 59114863 A 19840703 Showa
AI JP 1982-223681 (JP57223681 Showa) 19821222
PRAI JP 1982-223681 19821222
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1984
AB PURPOSE: To increase the specific dielectric constant of tantalum oxide by providing the primary tantalum film and the secondary tantalum film on an Si layer respectively at a specific vacuum degree and forming a tantalum oxide film by oxidizing the primary and secondary tantalum films.

CONSTITUTION: The primary Ta film is formed on the Si layer at a low vacuum degree of a value at 5×10<SP>-5</SP>Torr or more, and next the secondary Ta film is formed at a high vacuum degree of a value at 1×10<SP>-5</SP>Torr or less, which are thereafter oxidized, thus forming the Ta oxide film. Thereby, the specific dielectric constant of the Ta oxide increases because the oxide layer of the primary Ta film serves as a barrier against Si. Therefore, a Ta oxide film of a high dielectric constant can be formed on the Si layer, and can be utilized as the dielectric for a capacitor of an **MOS dynamic random access memory**, etc.

L29 ANSWER 20 OF 35 HCAPLUS COPYRIGHT 2003 ACS
AN 1984:415847 HCAPLUS
DN 101:15847
TI A corrugated capacitor cell (CCC)
AU Sunami, Hideo; Kure, Tokuo; Hashimoto, Norikazu; Itoh, Kiyoo; Toyabe, Toru; Asai, Shojiro
CS Cent. Res. Lab., Hitachi Ltd., Kokubunji, 185, Japan
SO IEEE Transactions on Electron Devices (1984), ED-31(6), 746-53
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
AB A new **MOS dynamic random access memory** (dRAM) cell named "CCC" was successfully developed based on a one-device cell concept. This CCC is characterized by an etched-moat storage-capacitor extended into the substrate, resulting in almost independent increase in storage capacitance CS of its cell size. A typical CS value of 60 fF was obtained with 3 .times. 7 .mu.m2 CCC having a 4-.mu.m deep moat and a capacitor insulator equiv. to 15 nm SiO2 in thickness. The CCC is discussed in terms of its capacitance characteristics, dRAM operation with unit 32-Kbit array, some limiting factors to its closer packing, and future considerations.

L29 ANSWER 21 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1983-F5747K [17] WPIX
DNN N1983-072572
TI MOS dynamic RAM of open bit line type - transfers electric charge stored in each MOS capacitor to bit line by turning on transfer gate.
DC U14
IN MASHIKO, M
PA (MITQ) MITSUBISHI DENKI KK
CYC 3
PI GB 2107544 A 19830427 (198317)* 15p
DE 3236729 A 19830511 (198320)
GB 2107544 B 19850530 (198522)
US 4520466 A 19850528 (198524)
DE 3236729 C 19880331 (198813)
ADT GB 2107544 A GB 1982-28899 19821008; DE 3236729 A DE 1982-3236729 19821004; US 4520466 A US 1982-432385 19820930
PRAI JP 1981-161608 19811009
AB GB 2107544 A UPAB: 19930925
The dynamic random access memory comprises a one-transistor type **MOS dynamic random access memory** of an open bit line type. This comprises two memory arrays at the left and the right sides of sense amplifying circuits. Each of both memory arrays comprises several memory cells and dummy cells, each of columns of memory cells and dummy cells having a cell plate voltage control circuit connected at the end thereof through a cell plate.

Each cell plate voltage control circuit is provided with a control signal having a level changing during a period when any of word lines or

dummy word lines is selected. It is responsive to selection of the word line or the dummy word line to discharge the voltage of the cell plate. It is also responsive to a change of the level of the control signal to charge the cell plate. Accordingly, transfer of a signal electric charge from the memory cell and the dummy cell to the bit line is performed at a high speed. Delay of the signal of the word line and the dummy word line is compensated, where a high speed operation can be performed.

L29 ANSWER 22 OF 35 JAPIO COPYRIGHT 2003 JPO
AN 1983-182863 JAPIO
TI SEMICONDUCTOR DEVICE
IN SHIMIZU SHINJI
PA HITACHI LTD
PI JP 58182863 A 19831025 Showa
AI JP 1982-65355 (JP57065355 Showa) 19820421
PRAI JP 1982-65355 19820421
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1983
AB PURPOSE: To suppress the variation in the noise, voltage in a C-**MOS dynamic random access memory** by forming a region such as a high impurity density at the deep position in the well, thereby effectively decreasing the well resistance.
CONSTITUTION: A C-MOS of a peripheral circuit is formed of an N-channel MISFET of P type well 5 and a P-channel MISFET on an epitaxial layer 4, and a memory array made of N-channel MISFET is formed of P type well 6. Alpha-ray intensity is increased due to the presence of wells 5, 6, and the latchup withstand voltage for the epitaxial well becomes sufficient. Since P<SP>+</SP> type buried layers 2, 3 of high impurity density are formed on the bottoms of the P type wells 5, 6, the well resistance is sufficiently decreased, thereby suppressing an electric noise at the operating time and the variation in the substrate voltage.

L29 ANSWER 23 OF 35 HCAPLUS COPYRIGHT 2003 ACS
AN 1982:519180 HCAPLUS
DN 97:119180
TI Integrated **MOSFET dynamic random access memories**
IN Ogura, Seiki; Tsang, Paul J.
PA International Business Machines Corp. , USA
SO Eur. Pat. Appl., 23 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 54117	A1	19820623	EP 1981-108126	19811009
	EP 54117	B1	19860723		
	R: DE, FR, GB				
	US 4366613	A	19830104	US 1980-217497	19801217
	JP 04118966	A2	19920420	JP 1990-255459	19900927
	JP 04180673	A2	19920626	JP 1990-255460	19900927
PRAI	US 1980-217497		19801217		

AB In a method of manufg. MOS FET random-access memories which is capable of delineating short (<1 .mu.m), lightly doped drain regions, n- regions are formed between the gate electrodes and field oxide insulators by ion implantation, and an insulator layer is then deposited. Reactive ion etching of the layer leaves narrow insulator regions adjacent to the gate electrode which protect portions of the n- regions during n+ implantation. These protected regions are the lightly doped source/drain regions.

01/21/2003

L29 ANSWER 24 OF 35 HCAPLUS COPYRIGHT 2003 ACS
AN 1982:628271 HCAPLUS
DN 97:228271
TI Analysis of soft error in MOS dynamic RAM
AU Yoshihara, Tsutomu; Takano, Satoshi; Taniguchi, Makoto; Harada, Hiroshi; Nakano, Takao
CS LSI Res. Dev. Lab., Mitsubishi Electr. Corp., Itami, 664, Japan
SO Denshi Tsushin Gakkai Ronbunshi, C (1982), J65-C(4), 251-6
CODEN: DTGCAY
DT Journal
LA Japanese
AB A theor. and exptl. study is presented on .alpha.-particle induced soft errors in a 64 kbt MOS dynamic RAM memory device. The relations between the soft errors and energy spectra of the incident .alpha.-particles, collection of generated charges, and crit. charge of the device were investigated. Assuming the distribution of the collected charges to be the Gaussian distribution, the soft errors are represented as a complimentary error function with respect to the crit. charge which is related to the source voltage. By exptl. detg. the soft-error dependence on the source voltage, the dispersion coeff. of the Gaussian distribution was detd. The expt. using a polyimide film showed that the dispersion coeff. largely depends on the incident energy and the soft-error improvement is the result of decrease in no. of .alpha.-particles due to absorption and in the dispersion coeff. due to energy dissipation. The exptl. data .alpha.-particle stopping power of the polyimide film is 1.47 .times. 103 times of that of air, and agrees well with the calcd. value.

L29 ANSWER 25 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1981-B4397D [07] WPIX
TI MOS random-access memory - has capacitive storage cells coupled along pairs of bit-line halves and to sensing amplifiers.
DC U14
IN HOLT, W M; SIMONSEN, C J; TSANG, S K
PA (ITLC) INTEL CORP
CYC 2
PI US 4247917 A 19810127 (198107)*
DE 3030994 A 19810319 (198113)
DE 3030994 C 19890928 (198939)
ADT DE 3030994 A DE 1980-3030994 19800816
PRAI US 1979-70132 19790827
AB US 4247917 A UPAB: 19930915
The **MOS dynamic random-access memory** (RAM) employs single transistor cells employing capacitive storage coupled to folded bit-line halves. These bit-line halves are connected to sense amplifiers employing cross-coupled transistors. Boosting circuits employing a variable capacitance are coupled to the bit-line halves to boost the potential on a line during reading.

The capacitor associated with each of the memory cells is coupled to a potential which is greater than the power supply potential. This plate potential is constant, independent of power supply variations and is internally generated. The dummy cells employed within the RAM are charged to a constant potential which does not vary with power supply variations.

L29 ANSWER 26 OF 35 HCAPLUS COPYRIGHT 2003 ACS
AN 1982:172698 HCAPLUS
DN 96:172698
TI New positive photoresist for critical dimension control
AU Kadota, Kazuya; Taki, Youichi; Shimizu, Shinji
CS Musashi Works, Hitachi Ltd., Tokyo, 187, Japan
SO Proceedings of SPIE-The International Society for Optical Engineering

(1981), 275(Semicond. Microlithogr. 6), 173-81
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB New pos. photoresists, AZ-1450J, HPR-204, and OFPR-800 were studied to minimize linewidth precision of **MOS dynamic random-access memories** (RAMs) using 1:1 scanning projection systems. To optimize resist linewidth characteristics of the new materials, striation, chem. stability, wet developing, and resistance for new dry etching were evaluated for each material. The availability was confirmed by application to the test device for an MOS dynamic RAM. This includes 128 .times. 10 transistor arrays with various channel lengths. The channel length variation decreased within 0.1 .mu.m (3.sigma.); and the threshold voltage variation was .+-.50 mV (3.sigma.) or less for 2-.mu. lines using AZ-1450J and OFPR-800.

L29 ANSWER 27 OF 35 HCAPLUS COPYRIGHT 2003 ACS
AN 1980:417916 HCAPLUS
DN 93:17916
TI Semiconductor device fabrication
IN Mochizuki, Itaru
PA Cho LSI Gijutsu Kenkyu Kumiai, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 55011359	A2	19800126	JP 1978-84206	19780711
PRAI	JP 1978-84206		19780711		

AB The fabrication steps are claimed for multilayer-wired semiconductor devices (CCD, **MOS, dynamic random-access memory**) employing improved electrode wiring.

L29 ANSWER 28 OF 35 HCAPLUS COPYRIGHT 2003 ACS
AN 1980:225309 HCAPLUS
DN 92:225309
TI Semiconductor device fabrication
IN Maeda, Tetsu
PA Cho LSI Gijutsu Kenkyu Kumiai, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 55008062	A2	19800121	JP 1978-80761	19780703
PRAI	JP 1978-80761		19780703		

AB A method for prepg. semiconductor devices having 2-layer gate electrodes is claimed, which allows the formation of a semiconductor device having a desired insulation breakdown voltage between the 2nd gate electrode and the substrate semiconductor. The method is esp. useful for prepg. **MOS dynamic** RAM (**random-access memory**)-type devices.

L29 ANSWER 29 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1978-B0870A [05] WPIX
TI **MOS dynamic random access memory** - has bistable flip-flop sensing amplifier connected

between bit line portions.
DC U14
IN BOETTCHER, C E; KARP, J A; REED, J A
PA (NASC) NAT SEMICONDUCTOR INC
CYC 1
PI US 4069474 A 19780117 (197805)*
PRAI US 1976-677462 19760415
AB US 4069474 A UPAB: 19930901
In a memory circuit, first and second bit line portions, each having a number of coupled memory cells, are provided for reading and writing electrical potentials into and out of the coupled memory cells. A bistable flip-flop type sensing amplifier is coupled between the first and second bit portion for sensing the voltage difference there between and for latching into one of the two states in response to sensing either a '0' or a '1' accessed to one of the bit line portions from an addressed memory cell to be read out of the memory.
A high input impedance amplifier is provided between the respective bit line portion and the respective input terminal of the sensing amplifier for isolating (buffering) the stray capacitance of the sensing amplifier circuit from the capacitance of its bit line.

L29 ANSWER 30 OF 35 JAPIO COPYRIGHT 2003 JPO
AN 1978-058736 JAPIO
TI INPUT/OUTPUT CONTROL SYSTEM FOR **MOS DYNAMIC RANDOM ACCESS MEMORY**
IN FURUYAMA TORU; OUCHI KAZUNORI
PA TOSHIBA CORP
PI JP 53058736 A 19780526 Showa
AI JP 1976-133908 (JP51133908 Showa) 19761108
PRAI JP 1976-133908 19761108
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1978
AB PURPOSE: To shorten the access time by omitting the processs to invert a stabilized state, by delaying the timing with which a sense circuit is driven in a writing cycle.
COPYRIGHT: (C)1978,JPO&Japio

L29 ANSWER 31 OF 35 HCAPLUS COPYRIGHT 2003 ACS
AN 1980:86823 HCAPLUS
DN 92:86823
TI The BO-MOS RAM cell
AU Sakurai, Junji
CS Fujitsu Ltd., Kawasaki, 211, Japan
SO Technical Digest - International Electron Devices Meeting (1978) 197-200
CODEN: TDIMD5; ISSN: 0163-1918
DT Journal
LA English
AB A new structure and its fabrication for **MOS dynamic** RAM (**random access memory**) cells are described. The buried oxide MOS RAM(BO-MOS RAM) cell consists of a planar MOS transfer gate and a buried storage capacitor of N+ diffusion. Its operation is identical to that of the conventional one-transistor dynamic RAM cell. The resulting advantages are: (a) a cell size of 6F2 with the min. lithog. feature size F achieved, which is equiv. to one-fifth to one-eighth of the conventional 16 or 64 Kbit RAM cell, (b) a combination of the smaller cell size and an elimination of the MOS capacitor should result in higher prodn. yield as well as higher packing d. in one-transistor dynamic RAM.

L29 ANSWER 32 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1977-C3039Y [11] WPIX
TI Select line hold down circuit for MOS memory decoder - includes selection

MOSFET and feedback MOSFET connected to NOR gate.
DC U14
PA (MOTI) MOTOROLA INC
CYC 1
PI US 4011549 A 19770308 (197711)*
PRAI US 1975-609855 19750902
AB US 4011549 A UPAB: 19930901
A decoder for a semiconductor **MOS random access memory** includes a **dynamic** NOR gate having a first output. The decoder also includes a selection MOSFET for providing a selection signal to a selection conductor connected to a row or column of an array of storage cells of said. random access memory.
The gate electrode of the selection MOSFET is connected to the output node of the NOR gate. The drain of the selection MOSFET is connected to a signal conductor adapted to having a signal applied thereto which is a function of a read/write signal applied to the random access memory. The source of the selection MOSFET is connected to the selection conductor.

L29 ANSWER 33 OF 35 JAPIO COPYRIGHT 2003 JPO
AN 1977-138847 JAPIO
TI **MOS DYNAMIC RANDOM ACCESS MEMORY**
IN JIYON EI RIIDO
PA NAT SEMICONDUCTOR CORP
PI JP 52138847 A 19771119 Showa
AI JP 1977-36888 (JP5236888 Showa) 19770331
PRAI US 1976-677461 19760415
SO INPADOC

L29 ANSWER 34 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1976-J2402X [37] WPIX
TI High density MOS integrated circuit memory array - uses single device dynamic cells and uniquely controlled sense amplifier.
DC U14
PA (ITLC) INTEL CORP
CYC 3
PI US 3978459 A 19760831 (197637)*
DE 2614297 A 19761104 (197646)
FR 2309014 A 19761223 (197708)
PRAI US 1975-569927 19750421
AB US 3978459 A UPAB: 19930901
The **MOS dynamic random-access memory** employs a number of sense lines coupled to several sense amplifiers. At least one transistor in each of the sense amplifiers is coupled between a source of potential and a sense line. A signal generator coupled to each of the sense amplifiers is used for causing the transistor of each of the sense amplifiers to sequentially charge the sense lines, and also to operate as a load for the amplifier.
Thus, a single transistor performs a precharging function in addition to acting as a load to the sense amplifier. A single noise suppression circuit provides planar noise suppression, the circuit is clocked with the same signals used to control the sense amplifier.

L29 ANSWER 35 OF 35 WPIX (C) 2003 THOMSON DERWENT
AN 1974-A4467V [12] WPIX
TI Buffer peripheral circuits - for interfacing **MOS dynamic random access memories** with TTL logic circuits.
DC U21 U22
PA (MOTI) MOTOROLA INC
CYC 1

01/21/2003

PI   US 3796893   A 19740312 (197412)*
PRAI US 1972-284183   19720828; US 1973-417151   19731119

01/21/2003

L39 ANSWER 1 OF 21 HCAPLUS COPYRIGHT 2003 ACS DUPLICATE 1
AN 2002:6359 HCAPLUS
DN 136:62581
TI Doping fabrication of dual work-function **MOSFETs** with borderless diffusion contacts for high-performance embedded **DRAM** technology
IN Mandelman, Jack A.; Dyer, Thomas Walter
PA International Business Machines Corp., USA
SO U.S., 20 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6335248	B1	20020101	US 2001-845665	20010430
PRAI	US 2001-845665		20010430		

AB The present invention provides a method for forming dual work-function **metal oxide semiconductor** field effect **transistors** (**MOSFETs**) which uses processing steps that solve the problem of doping the dual work function **MOSFETs**, while providing contacts to the diffusion regions which are borderless to the **gate conductors**. Specifically, the present invention provides a method wherein a self-aligned insulating gate cap is formed on top of a previously defined and doped **gate conductor** region. The inventive method which forms an insulating cap that is self-aligned to an underlying **gate conductor** enables the formation of dual work-function **gate conductors** and borderless diffusion contacts without the need of employing sep. block masks as required by prior art processes.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 2 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:10832 HCAPLUS
DN 136:78447
TI Single sided buried strap for a storage capacitor
IN Divakaruni, Ramachandra; Mandelman, Jack A.; Bergner, Wolfgang; Bronner, Gary B.; Gruening, Ulrike; Kudelka, Stephen; Michaelis, Alexander; Nesbit, Larry; Radens, Carl J.; Schloesser, Till; Tews, Heomut Horst
PA Infineon Technologies North America Corp., USA; International Business Machines Corporation
SO PCT Int. Appl., 37 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002001607	A2	20020103	WO 2001-US20206	20010625
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
	US 6426526	B1	20020730	US 2001-870068	20010530
PRAI	US 2000-603442	A	20000623		

AB A method for clearing an isolation collar from a 1st interior surface of a deep trench at a location above a storage capacitor while leaving the isolation collar at other surfaces of the deep trench. A barrier material is deposited above a node conductor of the storage capacitor. A layer of Si is deposited over the barrier material. Dopant ions are implanted at an angle into the layer of deposited Si within the deep trench, thereby

leaving the deposited Si un-implanted along 1 side of the deep trench. The un-implanted Si is etched. The isolation collar is removed in locations previously covered by the un-implanted Si, leaving the isolation collar in locations covered by the implanted Si.

L39 ANSWER 3 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:794068 HCAPLUS
DN 137:303288
TI TTO nitride liner for improved collar protection and TTO reliability
IN Divakaruni, Rama; Dyer, Thomas W.; Malik, Rajeev; Mandelman, Jack A.; Jaiprakash, V. C.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002149047	A1	20021017	US 2001-832605	20010411
PRAI	US 2001-832605		20010411		

AB A structure and method which enables the deposit of a thin nitride liner just before trench top oxide (TTO) high d. plasma (HDP) deposition during the formation of a vertical **MOSFET DRAM** cell device. This liner is subsequently removed after TTO sidewall etch. One function of this liner is to protect the collar oxide from being etched during the TTO oxide sidewall etch and generally provides lateral etch protection which is not realized in the current processing scheme. The process sequence does not rely on previously deposited films for collar protection, and decouples TTO sidewall etch protection from previous processing steps to provide addnl. process flexibility, such as allowing a thinner strap cut mask nitride and greater nitride etching during node nitride removal and buried strap nitrided interface removal. The presence of the nitride liner beneath the TTO reduces possibility of TTO dielec. breakdown between the gate and capacitor node electrode of the vertical **MOSFET DRAM** cell, while assuring strap diffusion to **gate conductor** overlap.

L39 ANSWER 4 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:522574 HCAPLUS
DN 137:71570
TI Fabrication of vertical **MOSFET** in forming **DRAM**
IN Divakaruni, Ramachandra; Lee, Heon; Mandelman, Jack A.; Radens, Carl J.; Sim, Jai-hoon
PA USA
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002090780	A1	20020711	US 2001-757514	20010110
	US 6414347	B1	20020702	US 2001-790011	20010209
	US 2002089007	A1	20020711		
	JP 2002222873	A2	20020809	JP 2001-388866	20011221
PRAI	US 2001-757514	A3	20010110		

AB An improved process for making a vertical **MOSFET** structure comprising: A method of forming a semiconductor memory cell array structure comprising: providing a vertical **MOSFET DRAM** cell structure having a deposited **gate conductor** layer

planarized to a top surface of a trench top oxide on the overlying **silicon** substrate; forming a recess in the **gate conductor** layer below the top surface of the **silicon** substrate; implanting N-type dopant species through the recess at an angle to form doping pockets in the array P-well; depositing an oxide layer into the recess and etching said oxide layer to form spacers on sidewalls of the recess; depositing a **gate conductor** material into said recess and planarizing said **gate conductor** to said top surface of the trench top oxide.

L39 ANSWER 5 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:502866 HCAPLUS
DN 137:55999
TI Fabrication of vertical **MOSFETs** for use in **DRAM** cells
IN Divakaruni, Ramachandra; Lee, Heon; Mandelman, Jack A.; Radens, Carl J.; Sim, Jai-hoon
PA International Business Machines Corporation, USA
SO U.S., 10 pp., Division of U.S. Ser. No. 757,514.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6414347	B1	20020702	US 2001-790011	20010209
	US 2002089007	A1	20020711		
	US 2002090780	A1	20020711	US 2001-757514	20010110
PRAI	US 2001-757514	A3	20010110		

AB An improved process is described for making a vertical **MOSFET** structure used in semiconductor memory cell arrays. The method comprises: providing a vertical **MOSFET DRAM** cell structure having a deposited **gate conductor** layer planarized to a top surface of a trench top oxide on the overlying **silicon** substrate; forming a recess in the **gate conductor** layer below the top surface of the **silicon** substrate; implanting N-type dopant species through the recess at an angle to form doping pockets in the array P-well; depositing an oxide layer into the recess and etching said oxide layer to form spacers on sidewalls of the recess; depositing a **gate conductor** material into said recess and planarizing said **gate conductor** to said top surface of the trench top oxide.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 6 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:39623 HCAPLUS
DN 136:111138
TI Structure and process for 6F2 trench capacitor **DRAM** cell with vertical **MOSFET** and 3F bitline pitch
IN Mandelman, Jack A.; Divakaruni, Ramachandra; Radens, Carl J.; Gruening, Ulrike
PA International Business Machines Corporation, USA
SO U.S., 39 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6339241	B1	20020115	US 2000-602426	20000623
	JP 2002026147	A2	20020125	JP 2001-189079	20010622

PRAI US 2000-602426 A 20000623

AB A memory cell structure is presented including a planar semiconductor substrate. A deep trench is in the semiconductor substrate. The deep trench has a plurality of side walls and a bottom. A storage capacitor is at the bottom of the deep trench. A vertical transistor extends down at least one side wall of the deep trench above the storage capacitor. The transistor has a source diffusion extending in the plane of the substrate adjacent the deep trench. An isolation extends down at least one other sidewall of the deep trench opposite the vertical transistor. Shallow trench isolation regions extend along a surface of the substrate in a direction transverse to the sidewall where the vertical transistor extends. A **gate conductor** extends within the deep trench. A wordline extends over the deep trench and is connected to the **gate conductor**. A bitline extends above the surface plane of the substrate and has a contact to the source diffusion between the shallow trench isolation regions.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 7 OF 21 WPIX (C) 2003 THOMSON DERWENT
AN 2002-656007 [70] WPIX
DNN N2002-518469 DNC C2002-184155
TI Memory array production for semiconductor memory devices, involves forming double gated vertical **MOSFETs** in deep trenches of substrate.
DC L03 U11 U12 U13 U14
IN BRONNER, G B; DIVAKARUNI, R; MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 2002094619 A1 20020718 (200270)* 24p
ADT US 2002094619 A1 US 2001-766013 20010118
PRAI US 2001-766013 20010118
AB US2002094619 A UPAB: 20021031

NOVELTY - Double gated vertical **MOSFETs** are formed in deep trenches of a **silicon** substrate (10) with exposed **gate conductors** (85). Wordlines (95) are formed in column direction over the **MOSFETs**, in contact with the exposed **gate conductors**. Bit lines are formed orthogonal to word lines and isolation trenches deeper than abutting bitline diffusion regions are formed in the trenches.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a memory cell array.

USE - For semiconductor memory devices such as **embedded dynamic random access memory** (**EDRAM**) cells.

ADVANTAGE - Provides a memory cell that is scalable below a minimum feature size of ca. 110 microns m, considerably eliminating back gating due to adjacent wordline and is also immune to the floating-well effects. Provides a memory cell where the **MOSFETs** and the isolation regions are self-aligned to the wordlines and bitlines of the cell. Allows continuity to the upper portion of the well and avoids floating well condition as the isolation regions are etched to a depth which is slightly deeper than the bitline diffusion regions. Exhibits much stronger gate control, leading to increased on-current, reduced short channel effects and reduced substrate sensitivity. By minimizing the distance between adjacent deep trenches, the memory cell can operate in a fully depleted state.

DESCRIPTION OF DRAWING(S) - The figure shows a view that illustrates processing steps of a memory cell.

Silicon substrate 10
Exposed **gate conductors** 85
Word lines 95

Spacers 160
Dwg.14B/14

L39 ANSWER 8 OF 21 WPIX (C) 2003 THOMSON DERWENT
AN 2003-027928 [02] WPIX
CR 2002-626871 [67]; 2002-641593 [69]
DNN N2003-021832 DNC C2003-006396
TI Semiconductor memory cell array structure production, e.g. **DRAM** structure, involves implanting N-type dopant species through recess in **gate conductor**, at specific angle to form N-type doping pockets.
DC L03 U11 U12 U13 U14
IN DIVAKARUNI, R; LEE, H; MANDELMAN, J A; RADENS, C J; SIM, J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6440793 B1 20020827 (200302)* 9p
ADT US 6440793 B1 US 2001-757514 20010110
PRAI US 2001-757514 20010110
AB US 6440793 B UPAB: 20030111
NOVELTY - N-type dopant species are implanted through a recess in a **gate conductor** layer on a trench top oxide (24) at a specific angle to form N-type doping pockets (46) in the array P-well. N+ doped **polysilicon** (22) is deposited into the recess. The deposited **polysilicon** is planarized to the top surface of the trench top oxide to form a **gate conductor**.

USE - For forming a semiconductor memory cell array structure such as a **dynamic random access memory** (**DRAM**) structure.

ADVANTAGE - As an additional spacer is provided between the bit line and the **gate conductor**, shorts between the diffusion stud and the **gate conductor** is reduced. As the bit line diffusion intersects only the gate surface of the **MOSFET**, the electrical potential barrier in the parasitic conduction path on the back surface of the **MOSFET** is increased. As the length of the diffusion is reduced, the drain induced barrier lowering is reduced. Hence, sensitivity of device electrical characteristics to variation in channel length of the vertical **MOSFET** is reduced. As the N-type doping pocket is self-aligned with the edge of the **gate conductor**, the variation in gate to diffusion overlap capacitance is prevented. Reduces surface state concentration, as the N-type dopant species is implanted at a specific angle.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the production of a vertical **MOSFET**.

N+ doped **polysilicon** 22
Trench top oxide 24
N-type doping pockets 46
Dwg.9/10

L39 ANSWER 9 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:168273 HCAPLUS
DN 134:201605
TI Disposable spacers in fabrication of **MOSFET** gate structure
IN Akatsu, Hiroyuki; Divakaruni, Ramachandra; Lee, Gill Young
PA Infineon Technologies North America Corp., USA; International Business Machines Corporation
SO PCT Int. Appl., 17 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO. KIND DATE APPLICATION NO. DATE

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PI    WO 2001017010     A1    20010308       WO 2000-US23850  20000830
      WO 2001017010     C2    20020919
          W:  CN, JP, KR
          RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,
              PT, SE
      US 6281084        B1    20010828       US 1999-386832   19990831
PRAI  US 1999-386832    A     19990831
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AB There is disclosed the process of forming a **gate conductor** for a semiconductor device. The process begins with the step of providing a semiconductor substrate having a gate stack formed thereon, the gate stack including a sidewall. Dielec. spacers are formed on the **gate conductor** sidewalls, the dielec. spacers comprising an inner spacer (36) and an outer spacer (38), the outer spacer being of a doped glass material. Ions are implanted into the semiconductor substrate outwardly of the dielec. spacers. The outer spacers are then removed.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 10 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:668376 HCAPLUS
DN 135:219715
TI Structure and process for fabricating a 6F2 **DRAM** cell having vertical **MOSFET** and large trench capacitance
IN Mandelman, Jack A.; Divakaruni, Rama; Radens, Carl
PA International Business Machines Corporation, USA
SO U.S., 24 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

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      PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
      ---------------  ----  --------       ---------------  --------
PI    US 6288422        B1    20010911       US 2000-540276   20000331
PRAI  US 2000-540276          20000331
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AB The present invention relates to dense memory cells, and more particular to 6F2 memory cells which are scalable to a min. feature size of 100 nm or below. The present invention is also directed to a process of fabricating such a memory cell which avoids lithog. difficult features. The 6F2 memory cell structure comprises a plurality of capacitors each located in a sep. trench in a substrate; a plurality of transfer transistors each having a vertical gate dielec., a **gate conductor**, and a bitline diffusion, each transistor being located above and elec. connected to a resp. trench capacitor; a plurality of troughs in a striped pattern about the transistor, the troughs being spaced apart by a substantially uniform spacing, the plurality of striped troughs comprising a 1st group of troughs consisting of every other trough being filled with a dielec. material, and a 2nd group of troughs being the remaining troughs of the plurality, the 2nd group of troughs contg. dielec. material, damascened wordlines and damascene wordline contacts; a resp. wordline elec. contact connected to each resp. **gate conductor**; and a bitline contacted to each bitline diffusion, in which the bitline diffusions have a width defined by the spacing of the striped troughs and each wordline elec. contact is self-aligned to an edge of a trough of the 2nd group of troughs.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 11 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:630920 HCAPLUS

01/21/2003

DN 135:188769
TI Structure and process for 6F2 DT cell having vertical **MOSFET** and
large storage capacitance
IN Mandelman, Jack A.; Divakaruni, Rama
PA International Business Machines Corporation, USA
SO U.S., 24 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6281539	B1	20010828	US 2000-540854	20000331
PRAI	US 2000-540854		20000331		

AB A 6F2 memory cell comprising a plurality of capacitors each located in a sep. trench that is formed in a semiconductor substrate; a plurality of transfer transistors each having a vertical gate dielec., a **gate conductor**, and a bitline diffusion, each transistor is located above and elec. connected to a resp. trench capacitor; a plurality of dielec.-filled isolation trenches in a striped pattern about the transistors, the isolation trenches are spaced apart by a substantially uniform spacing; a resp. wordline elec. contacted to each resp. **gate conductor**, the wordline is in the same direction as the isolation stripes; and a bitline in contact with the bitline diffusion, in which the bitline diffusions have a width that is defined by the spacing of the isolation trenches.

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 12 OF 21 WPIX (C) 2003 THOMSON DERWENT
AN 2001-450371 [48] WPIX
DNN N2001-333330 DNC C2001-135968
TI Formation of **dynamic random access memory** array and support **metal oxide semiconductor** field effect **transistors** involves saliciding tops of bitline diffusion stud landing pad in array and **gate conductors** for support transistors.
DC L03 U11
IN DIVAKARUNI, R; GRUENING, U; MANDELMAN, J A; RUPP, T S; MANDELMAN, J; RUPP, T
PA (IBMC) INT BUSINESS MACHINES CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP
CYC 23
PI US 6258659 B1 20010710 (200148)* 12p
WO 2002045130 A2 20020606 (200238) EN
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: CN JP KR
KR 2002042420 A 20020605 (200277)
ADT US 6258659 B1 US 2000-725412 20001129; WO 2002045130 A2 WO 2001-US44625 20011128; KR 2002042420 A KR 2001-70618 20011114
PRAI US 2000-725412 20001129
AB US 6258659 B UPAB: 20010829
NOVELTY - Formation of memory array and support transistors comprises applying a block mask to protect supports while stripping nitride layer from array and etching exposed **polysilicon** layer to the top of gate oxide layer and to form bitline diffusion stud landing pad in array and **gate conductors** for the support transistors; and saliciding the tops of the landing pad and the **gate conductors**.

DETAILED DESCRIPTION - Formation of memory array and support transistors comprises forming a trench capacitor in a **silicon**

substrate (11) having a gate oxide layer (18), **polysilicon** layer, and top dielectric nitride layer. A patterned mask is applied over the array and support areas. Recesses are formed in the nitride layer, **polysilicon** layer and shallow trench isolation region (14). A silicide and an oxide cap are formed in the recesses in the nitride layer, **polysilicon** layer and shallow trench isolation region. A block mask is applied to protect the supports while stripping the nitride layer from the array. The exposed **polysilicon** layer is etched to the top of the gate oxide layer. The nitride layer is stripped from the support region and a **polysilicon** layer is deposited over the array and support areas. A mask is applied to pattern and forms a bitline diffusion stud landing pad in the array and **gate conductors** (28) for the support transistors. The tops of the landing pad and the **gate conductors** are salicided. An interlevel oxide layer (36) is applied and then vias in the interlevel oxide layer are opened for establishing conductive wiring channels.

USE - For forming **dynamic random access memory** (**DRAM**) array and support **metal oxide semiconductor** field effect **transistors** (**MOSFETs**).

ADVANTAGE - The method fabricates very high-density embedded **DRAM** and very high-performance support **MOSFETs**. It provides for a bitline contact self-aligned to the active area, eliminates boron-phosphosilicate glass reflow step, reduces thermal budget, and allows shallower source/drains.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **DRAM** array and support **MOSFET** at a production stage.

Silicon substrate 11
Shallow trench isolation region 14
Gate oxide layer 18
Gate conductors 28
Interlevel oxide layer 36

Dwg.18/18

L39 ANSWER 13 OF 21 WPIX (C) 2003 THOMSON DERWENT
AN 2001-501683 [55] WPIX
CR 2001-315686 [32]
DNN N2001-371997
TI Trench capacitor type **DRAM** cell has vertical **metal oxide semiconductor** field effect **transistor** transfer device in upper portion of deep trenches and collar isolation oxide in upper portion on deep trench side walls.
DC U13 U14
IN FURUKAWA, T; HAKEY, M C; HORAK, D V; MA, W H; MANDELMAN, J A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6184549 B1 20010206 (200155)* 10p
ADT US 6184549 B1 Div ex US 1998-86057 19980528, US 1999-296807 19990423
PRAI US 1998-86057 19980528; US 1999-296807 19990423
AB US 6184549 B UPAB: 20010927

NOVELTY - Deep trenches (74,75,74',75') are formed in p type substrate with lower portion partially filled with n+ **polysilicon** storage node and surrounded by n+ **silicon** storage plate. Vertical **MOSFET** transfer device is formed in upper portion of trenches. A collar isolation oxide is formed in upper portion on deep trench side walls between n+ buried strap diffusion of **MOSFET** and storage plate.

DETAILED DESCRIPTION - A recessed **polysilicon** conductor is provided within upper portion of deep trenches gating and p type **silicon** adjacent deep trench. A **gate conductor**

connects an n+ bit line diffusion (65) formed above p type **silicon** and n+ buried strap diffusion. Several recessed active and passive wordline conductors are formed on insulating layer above trenches.
USE - Trench capacitor type integrated circuit **dynamic random access memory**.
ADVANTAGE - Byintegrating robust transfer device in **dynamic random access memory** cell with shallow trench isolation region constructed between adjacent trench capacitor cells, the device channel length requirement is made independent of cell size, thus the dimension of device can be reduced. Using square printing to form shallow trench isolation and detrenches, scaling of the cell to very small dimensions is allowed.
DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of trench capacitor type **DRAM** cell.
Line diffusion 65
Deep trenches 74,75,74',75'
Dwg.9/11

L39 ANSWER 14 OF 21 WPIX (C) 2003 THOMSON DERWENT
AN 2000-637353 [61] WPIX
DNN N2000-472650
TI **Metal oxide semiconductor** field effect **transistor** of **DRAM**, has gate dielectric formed under outer conductors with greater thickness than under central conductor for reducing gate induced drain leakage.
DC U11 U12
IN MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6097070 A 20000801 (200061)* 10p
ADT US 6097070 A US 1999-250881 19990216
PRAI US 1999-250881 19990216
AB US 6097070 A UPAB: 20001128
NOVELTY - Gate dielectrics (27,28) are formed over substrate having gate channel area (20), and source and drain areas (21). Central conductors (25) of P-type **polysilicon** above channel and outer conductors (26) of N-type **polysilicon** over dielectrics, are separated by the dielectrics. The dielectric (28) under conductors (26) has thickness greater than that under conductor (25) for reducing gate induced drain leakage.
DETAILED DESCRIPTION - A conductive silicide layer (23) is formed on conductors for electrically connecting them. An INDEPENDENT CLAIM is also included for integrated circuit structure forming process.
USE - For e.g. NMOSFET, PMOSFET used for low power applications e.g. low power **dynamic random access memory** (**DRAM**).
ADVANTAGE - Since the gate dielectric thickness under the central **gate conductor** and under the outer conductors are independently specified, the gate induced drain leakage is reduced which is valuable for low power application.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic diagram of cross-sectional view of an integrated circuit.
Gate channel area 20
Drain areas 21
Conductive silicide layer 23
Central conductors 25
Outer conductors 26
Gate dielectric 27,28
Dwg.2/5

L39 ANSWER 15 OF 21 WPIX (C) 2003 THOMSON DERWENT

01/21/2003

AN 2000-603752 [58] WPIX
DNN N2000-446830 DNC C2000-180772
TI **Dynamic random access memory** (
DRAM) for use in semiconductor devices includes complementary transistors in the support circuitry with dual work-function gates.
DC L03 U11 U12 U13 U14
IN ALSMEIER, J; TOBBEN, D; TOEBBEN, D
PA (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (INFN) INFINEON NORTH AMERICA CORP
CYC 30
PI EP 1039533 A2 20000927 (200058)* EN 14p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000311991 A 20001107 (200061) 43p
CN 1268772 A 20001004 (200067)
US 6235574 B1 20010522 (200130)
KR 2001006849 A 20010126 (200152)
TW 448543 A 20010801 (200222)
ADT EP 1039533 A2 EP 2000-103620 20000221; JP 2000311991 A JP 2000-80366 20000322; CN 1268772 A CN 2000-104703 20000322; US 6235574 B1 Div ex US 1999-273402 19990322, US 2000-568064 20000510; KR 2001006849 A KR 2000-14498 20000322; TW 448543 A TW 2000-105166 20000426
PRAI US 1999-273402 19990322; US 2000-568064 20000510
AB EP 1039533 A UPAB: 20010914

NOVELTY - A **dynamic random access memory** (**DRAM**) comprises complementary transistors in the support circuitry having dual work-function gates.

DETAILED DESCRIPTION - A **dynamic random access memory** (**DRAM**) comprises a **silicon** chip having a central area forming an array of memory cells with n-channel **metal oxide semiconductor** field effect **transistors** (N-**MOSFETs**), and a peripheral area forming the support circuitry including both the N-**MOSFETs** and p-channel **metal oxide semiconductor** field effect **transistors** (P-**MOSFETs**). The N-**MOSFETs** in the memory cells use N-doped polycide gates. The N- and P-**MOSFETs** in the support circuitry use N- and P-doped **polysilicon** gates.

INDEPENDENT CLAIMS are also included for:

(1) a method for forming a **DRAM** comprising (i) forming a masking layer of **silicon** oxide over the surface of the chip area and removing the layer from the central area where the memory cell arrays are to be included, but leaving it in place in the peripheral portion where the support circuitry is to be included; (ii) forming the N-**MOSFETs** of the memory cells in the central area and including N-**MOSFET gate conductors** (40A-B) that include an underlying **polysilicon** layer (14) that is doped with donor atoms and an overlying metal silicide layer; (iii) covering the chip area with a masking layer and removing it from the central area of the chip; (iv) removing the **silicon** oxide layer from the peripheral portion of the chip area; (v) covering the peripheral portion with a masking layer and removing it where N-**MOSFETs** are to be formed; (vi) forming the N-**MOSFETs** of the support circuitry in the peripheral portion and including N-**MOSFET gate conductors** as above; (vii) covering the peripheral area with a masking layer and removing it where P-**MOSFETs** are to be formed; and (viii) forming the P-**MOSFETs** of the support circuitry in the peripheral portion and including P-**MOSFET gate conductors** that include an underlying **silicon** layer that is doped with acceptor atoms and an overlying layer of a metal silicide; and

(2) a method for forming a stack that includes a monocrystalline

silicon p-type substrate.
USE - For use in semiconductor devices.
ADVANTAGE - The invention provides an improved performance.
DESCRIPTION OF DRAWING(S) - The figure shows a portion of a **silicon** chip in a **DRAM**.
Polysilicon layer 14
Gate conductors 40A-B
Salicide source and drain contacts 56A-B, 57-59
Dwg.17/17

L39 ANSWER 16 OF 21 WPIX (C) 2003 THOMSON DERWENT
AN 2000-226155 [20] WPIX
DNN N2000-169606 DNC C2000-069194
TI Manufacture of deep trench **DRAM** capacitor structure, comprises forming temperature sensitive high dielectric constant material on bottom electrode layer and lining sidewalls of storage trench region.
DC L03 U11 U12 U13 U14
IN JAMMY, R; MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 27
PI EP 987765 A2 20000322 (200020)* EN 19p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000091525 A 20000331 (200027) 17p
US 6222218 B1 20010424 (200125)
US 2001039087 A1 20011108 (200171)
US 6352892 B2 20020305 (200224)
ADT EP 987765 A2 EP 1999-113439 19990710; JP 2000091525 A JP 1999-259440 19990913; US 6222218 B1 US 1998-152835 19980914; US 2001039087 A1 Div ex US 1998-152835 19980914, US 2001-764656 20010117; US 6352892 B2 Div ex US 1998-152835 19980914, US 2001-764656 20010117
FDT US 2001039087 A1 Div ex US 6222218; US 6352892 B2 Div ex US 6222218
PRAI US 1998-152835 19980914; US 2001-764656 20010117
AB EP 987765 A UPAB: 20000426
NOVELTY - Fabricating a trench capacitor semiconductor memory structure comprises forming a temperature sensitive high dielectric constant material into the storage node of the **DRAM** trench capacitor.
DETAILED DESCRIPTION - Fabricating a trench capacitor semiconductor memory structure comprises:
(a) providing a semiconductor structure comprising a semiconductor substrate or wafer with at least one storage trench region and a raised shallow trench isolation (STI) region adjacent to the storage trench, the structure has preformed layers (16a,16b) of a partial **gate conductor** stack formed in the substrate or wafer which are spaced apart by the storage trench and raised STI regions;
(b) forming a bottom electrode layer (22) in the storage trench region;
(c) forming a temperature sensitive high dielectric constant material (24) on the bottom electrode layer and lining sidewalls of the storage trench region;
(d) forming a top electrode (26) over the dielectric material;
(e) filling the storage trench region with **polysilicon** (28);
(f) completing fabrication of a capacitor in the storage trench region;
(g) forming a patterned **gate conductor** region from the preformed **gate conductor** stack layers; and
(h) forming subsequent device connections.
An INDEPENDENT CLAIM is also included for a memory cell comprising a capacitor formed in a trench in a wafer, a **MOSFET** comprising at least a patterned **gate conductor** stack and

source/drain regions, the capacitor and the **MOSFET** being connected by a buried-strap outdiffusion region whose lateral outdiffusion is less than 50 nm, preferably 15-30 nm.

USE - Semiconductor memory device, particularly deep trench **DRAM** capacitor structure.

ADVANTAGE - In the process, the buried-strap outdiffusion from the trench storage capacitor does not encounter the STI liner oxidation, sacrificial oxidation and gate oxidation steps. This limits the thermal budget and the amount of buried-strap outdiffusion.

DESCRIPTION OF DRAWING(S) - The drawing shows a process step of the invention.

Preformed **gate conductor** layers 16a,16b
Bottom electrode 22
Temperature sensitive high dielectric constant material 24
Top electrode 26
Polysilicon 28
Oxide 30
Polysilicon 32
Dwg.31/4

L39 ANSWER 17 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:651029 HCAPLUS
DN 132:17624
TI Poly gate depletion effect on deep sub-micrometer CMOS
AU Ye, Qiuyi; Limb, Young; Berry, Wayne; Li, Yujun; Thanh, Liem Do; Rengarajan, R.; Tonti, W.
CS Infineon Technologies Corp., Hopewell Junction, NY, 12533, USA
SO Proceedings - Electrochemical Society (1999), 99-18(ULSI Process Integration), 301-310
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB As CMOS feature size is scaled into the 0.1 .mu.m regime many old problems become new challenges requiring innovative solns. and novel characterization means. The **polysilicon gate conductor** (PGC) depletion effect falls into this category and has recently gained much attention. In this paper we study the PGC effect on n-channel **MOSFET**'s fabricated in a 0.175.mu.m **DRAM** technol. Phys. gate oxide thickness, PGC depletion, and the active PGC doping d. (Nactive) is detd. through C-V measurement. Transmission Electron Microscopy is used to uncover the PGC microstructure near the PGC/SiO2 interface. In our process Nactive is defined by two unique high temp. process steps: (1) the highest temp. step (> 1000.degree.C), (Tmax), which establishes the PGC grain size, and (2) the final high temp. annealing step(> 700.degree.C) (Tfinal) which establishes PGC dopant segregation to grain boundary. The competing trade-off of a low CMOS thermal budget and thin gate oxide for maximized performance is contrasted with the higher thermal budgets of a non-depleted PGC are discussed. A device design process window is proposed to meet the competing requirements.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 18 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:334242 HCAPLUS
DN 129:61648
TI **MOSFET** IC device and fabrication thereof
IN Brasbramanyam, Kalanum; Brodsky, Stephen Bruce; Conti, Richard Anthony; Kare, Badi L.
PA International Business Machines Corp., USA

01/21/2003

SO Jpn. Kokai Tokkyo Koho, 19 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10135460	A2	19980522	JP 1997-293705	19971027
	US 5923999	A	19990713	US 1996-741159	19961029
	US 6114736	A	20000905	US 1999-351808	19990712
PRAI	US 1996-741159	A	19961029		

AB The invention relates to a **MOSFET** LSI, e.g., a **DRAM**, wherein the placement of a W nitride barrier prevents migration of dopant atoms in the **polysilicon** layer into the W silicide layer during the post **gate conductor** thermal cycling.

L39 ANSWER 19 OF 21 WPIX (C) 2003 THOMSON DERWENT
AN 1990-150706 [20] WPIX
DNN N1992-072652 DNC C1992-045126
TI Semiconductor device esp. for **dram** - has tungsten buried layer formed, flattened w.r.t gate electrode and gate constituting field shield.
DC L03 U11 U12 U13 U14
PA (MITQ) MITSUBISHI DENKI KK
CYC 2
PI JP 02094472 A 19900405 (199020)*
US 4994893 A 19910219 (199110)
US 5094965 A 19920310 (199213) 16p
ADT JP 02094472 A JP 1988-247670 19880929; US 4994893 A US 1989-405284 19890911; US 5094965 A US 1990-606276 19901031
PRAI JP 1988-247670 19880929

L39 ANSWER 20 OF 21 HCAPLUS COPYRIGHT 2003 ACS
AN 1986:506614 HCAPLUS
DN 105:106614
TI The effects of carbon on Czochralski **silicon** used for **dynamic random access memory** production
AU Craven, R. A.; Bailey, W. E.; Moody, J. W.; Falster, R. J.; Shive, L. W.
CS Monsanto Electron. Mater. Co., St. Louis, MO, 63167, USA
SO Materials Research Society Symposium Proceedings (1986), 59(Oxygen, Carbon, Hydrogen Nitrogen Cryst. Silicon), 359-65
CODEN: MRSPDH; ISSN: 0272-9172
DT Journal
LA English
AB Czochralski Si with const. controlled O level of 15+/-0.5 ppma (ASTM F121-80) and varying C content intentionally doped at 5 different levels from 0.1 to 4.1 ppma (ASTM F123-81) was used to fabricate 16 K dynamic RAMs, **MOS** test capacitors, with **guard rings**, and pn junctions. The results of the expts. were analyzed for relative yield to functional and refresh characteristics, **MOS** generation and bulk recombination lifetime, pn function leakage, and both surface and bulk defect densities. Peak performance of the Si did not occur at the lowest C level but was dominated by the O ppt. defect d. and depth of the denuded zone near the active device regions. The results of the capacitor measurements, dynamic RAM yield measurements, junction leakage measurements, and bulk and surface lifetime measurements are self-consistent and emphasize the need for control of the O pptn. whether it is nucleated by C or other homogeneous and heterogeneous processes. There is no evidence that C has any impact on device performance other than its impact on the pptn. kinetics of the interstitial O.

L39 ANSWER 21 OF 21 JAPIO COPYRIGHT 2003 JPO
AN 2002-222873 JAPIO
TI IMPROVED VERTICAL **MOSFET**
IN RAMACHANDORA DEIVAKARUNI; LEE HEON; MANDELMAN JACK A; RADENS CARL J; SIM JAI-HOON
PA INTERNATL BUSINESS MACH CORP <IBM>
PI JP 2002222873 A 20020809 Heisei
AI JP 2001-388866 (JP2001388866 Heisei) 20011221
PRAI US 2001-757514 20010110
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide an improved method of forming a vertical **MOSFET** structure.
SOLUTION: A method of forming a semiconductor memory cell array structure comprises a process of providing a vertical **MOSFET DRAM** cell structure having a deposited **gate conductor** layer 22 planarized up to the top surface of a trench top oxide 24 on a **silicon** substrate, a process of forming a recess 39 in the **gate conductor** layer below the top surface of the **silicon** substrate, a process of forming doping pockets 46 in an array P well 32 by implanting N-type dopant species through the recess at an angle, a process of forming spacers 44 on the side wall of the recess by depositing an oxide layer in the recess and then etching the oxide layer, and a process of depositing a **gate conductor** material in the recess and then planarizing the **gate conductor** material up to the top surface of the trench top oxide.

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01/21/2003

L41 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:616101 HCAPLUS
DN 137:162431
TI Open bit line **DRAM** with ultra thin body transistors
IN Forbes, Leonard; Ahn, Kie Y.
PA Micron Technology, Inc., USA
SO U.S. Pat. Appl. Publ., 31 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002109176	A1	20020815	US 2001-780125	20010209
PRAI	US 2001-780125		20010209		

AB Structures and method for an open bit line **DRAM** device are provided. The open bit line **DRAM** device includes an array of memory cells. Each memory cell in the array of memory cells includes a pillar extending outwardly from a semiconductor substrate. The pillar includes a single cryst. first contact layer and a single cryst. second contact layer sepd. by an oxide layer. In each memory cell a single cryst. vertical transistor is formed along side of the pillar. The single cryst. vertical transistor includes an ultra thin single cryst. vertical first source/drain region coupled to the first contact layer, an ultra thin single cryst. vertical second source/drain region coupled to the second contact layer, an ultra thin single cryst. vertical body region which opposes the oxide layer and couples the first and the second source/drain regions, and a gate opposing the vertical body region and sepd. therefrom by a gate oxide. A plurality of buried bit lines are formed of single cryst. semiconductor material and disposed below the pillars in the array memory cells for **interconnecting** with the first contact layer of column adjacent pillars in the array of memory cells. Also, a plurality of **word lines** are included. Each **word line** is disposed orthogonally to the plurality of buried bit lines in a trench between rows of the pillars for addressing gates of the single cryst. vertical transistors that are adjacent to the trench.

L41 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:556072 HCAPLUS
DN 137:118023
TI Method of automatically defining a landing via
IN Wu, King-Lung
PA Taiwan
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002098687	A1	20020725	US 2001-764331	20010119
	US 6429106	B2	20020806		
PRAI	US 2001-764331		20010119		

AB The present invention provides a method of automatically defining a landing via on a semiconductor wafer. The present invention involves first forming a conductive layer and a photoresist layer on the surface of the semiconductor wafer. Then, patterns of a plurality of **word lines** are defined on the surface of the photoresist layer, and patterns of a plurality of auxiliaries are defined around the area

predetd. to form the landing via between each two **word lines** on the surface of the photoresist layer. Thereafter, the patterned photoresist layer is used as a hard mask to etch the conductive layer to form each **word line** on the semiconductor wafer, and to simultaneously form the auxiliaries around the area predetd. to form the landing via. Finally, a plurality of spacers are formed around each **word line** and each auxiliary dovetail together to form a landing via hole and to automatically define the position of the landing via.

L41 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:551595 HCAPLUS
DN 137:102513
TI Method of making self-aligned bit-lines
IN Gau, Jing-Horng
PA United Microelectronics Corp., Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6423641	B1	20020723	US 2000-664428	20000918
PRAI	US 2000-664428		20000918		

AB The invention relates to a process for making self-aligned bit-lines on a **MOS** transistor **DRAM** integrated circuit. The semiconductor wafer comprises a **silicon** substrate, a plurality of **word-lines** located on the **silicon** substrate and a first dielec. layer that covers each **word-line**. A plurality of bit-line contacts are formed that are level with the surface of the first dielec. layer. A second dielec. layer is formed on the surface of the semiconductor wafer and a plurality of node contacts are formed in the second and first dielec. layer, which are leveled with the surface of the second dielec. layer. Portions of the second dielec. layer are removed to make the top portion of each node contact higher than the surface of the second dielec. layer. A spacer is formed around this top portion of each node contact. Finally, the top portion of each node contact and the spacer are used as hard masks to form a plurality of bit-lines in the second and first dielec. layers, and a plurality of bit-line contacts contact with every bottom portion of the bit-line.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:378149 HCAPLUS
DN 132:355710
TI Method for simultaneously fabricating a **DRAM** capacitor and metal **interconnections**
IN Yang, Fu-Liang; Jeng, Erik S.; Lin, Bih-Tiao; Lee, I-Ping
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6071789	A	20000606	US 1998-190054	19981110
PRAI	US 1998-190054		19981110		

AB A method for simultaneously forming a storage node and a plurality of **interconnection** in fabricating a semiconductor device on a substrate. The method comprises the steps of: forming a 1st dielec. layer over said cell array area and said periphery; forming a plurality of 1st contact holes through said 1st dielec. layer in said cell array area and said periphery area, said periphery area including a bitline and a **word line**, said **word line** and said bitline being used for addressing said memory cell;. Forming a 1st conductive layer in said plurality of 1st contact holes and on said 1st dielec. layer; patterning and etching said 1st conductive layer to form said storage node and said plurality of **interconnections** simultaneously; forming a 2nd dielec. layer and a 2nd conductive layer subsequently on said 1st dielec. layer, said storage node and said plurality of **interconnections**; and patterning and etching said 2nd dielec. layer and said 2nd conductive layer to form a charge storage means and a plurality of contact plugs.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:487168 HCAPLUS
DN 131:109922
TI **Word line** resistance reduction method and design for high-density memory device with relaxed metal pitch
IN Kirsch, Howard C.; Lu, Chih-yuan
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5933725	A	19990803	US 1998-85612	19980527
PRAI	US 1998-85612		19980527		

AB A method and design for stitching **polysilicon wordlines** to straps formed of **interconnected** metal line segments formed in two or more metalization levels. Each strap comprises a continuous conductive metal line passing alternatively from one metal layer to another in a selected sequence. The sequence of segments in each strap alternates in phase with the sequence in next nearest neighbor straps but may be in phase with second nearest neighbor straps. Thereby the pitch of strap segments on each metalization level is at least twice that of the subjacent **polysilicon wordlines**. The total length of each metal in each strap is the same in all straps. This arrangement allows the use of metals having different resistivities in each strap with all the straps having identical overall resistance. The metals used in the two or more levels may also have different min. design rules without compromising the identical overall performance of all the straps. In a second embodiment a method and design is described for doubling the length of **polysilicon** sub-**wordlines** in a sub-**wordline** memory array without reducing performance by connecting sub-**wordline** to sub-**wordline** decoders by metal straps connected to the sub-**wordlines** midpoints.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 6 OF 6 WPIX (C) 2003 THOMSON DERWENT
AN 1999-429692 [36] WPIX
DNN N1999-319876 DNC C1999-126588
TI Fabrication of capacitors with platinum electrodes for **dynamic**

random access memories (DRAMs).

DC L03 U11 U12 U13 U14
IN GRAETTINGER, T M; MCCLURE, B A; SCHUELE, P
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5930639 A 19990727 (199936)* 18p
ADT US 5930639 A US 1996-631290 19960408
PRAI US 1996-631290 19960408
AB US 5930639 A UPAB: 19990908

NOVELTY - The platinum electrodes are etched using physical ion etching with oxygen ions though a titanium nitride mask. Due to the high selectivity and since the titanium nitride is very thin and partially consumed in the etch there is no surface for redeposition to occur.

DETAILED DESCRIPTION - Forming a capacitor by:

(a) providing a noble metal film on semiconductor substrate (10);

(b) forming a metal nitride film over the noble metal;

(c) forming a bottom capacitor electrode (22) by etching the noble metal film with a physical ion etch process that etches the noble metal at a higher rate than the nitride;

(d) removing the remaining metal nitride;

(e) forming capacitor dielectric (24) over the bottom electrode;

(f) forming a noble metal film over the dielectric and a second nitride film over the metal; and

(g) etching the noble metal film with a physical ion etch that etches the metal at a higher rate than the nitride.

The physical ion etch is preferably with ionized oxygen, the noble metal is platinum and the nitride is titanium nitride.

USE - Fabrication of **DRAMs** and other memory devices.

ADVANTAGE - The noble metal films can be etched without the problem of redeposition and sloping sidewalls and capacitors can be formed with high capacitance, lower tolerances, greater device density, and less metal volume.

DESCRIPTION OF DRAWING(S) - The drawing shows a section of a **MOS** stacked memory structure.

L42 ANSWER 1 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:610540 HCAPLUS
DN 137:133098
TI Method of manufacturing embedded **DRAM**
IN Suen, Shr-Wei
PA United Microelectronics Corp., Taiwan
SO Taiwan, 16 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 395053	B	20000621	TW 1998-87116431	19981002
PRAI	TW 1998-87116431		19981002		

AB The method comprises: firstly, forming **word line** and gate in the memory region and the logic circuit region, then forming an etch stop layer; and then proceeding the memory cell **array** manuf. process in the memory region. Subsequently, removing the dielec. layer in the logic circuit region by etching and using the etch stop layer as the etching endpoint, and then removing the etch stop layer to expose the gate. Next, proceeding high-energy retrograde channel profile implantation through the gate of the logic circuit region, so as to form source/drain region on the substrate at both sides of the gate, resp., and form metal silicide on the source/drain region. The invention proceeds ion implantation after the manuf. process of the memory cell **array**, which can avoid the high-temp.-caused diffusion phenomena in the implantation region, and prevent the metal silicide from agglomeration at high temp.

L42 ANSWER 2 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:595266 HCAPLUS
DN 137:148776
TI Structure and method for a compact trench-capacitor **DRAM** cell with body contact
IN Mandelman, Jack A.; Radens, Carl J.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 26 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002105019	A1	20020808	US 2001-777576	20010205
PRAI	US 2001-777576		20010205		

AB A compact **DRAM** cell **array** that substantially minimizes floating-body effects and device-to-device interactions is disclosed. The compact **DRAM** cell **array** includes a plurality of annular memory cells that are arranged in rows and columns. Each annular memory cell includes a vertical **MOSFET** and an underlying capacitor that are in elec. contact to each other through a buried-strap out-diffusion region which is present within a portion of a wall of each annular memory cell such that the portion partially encircles the wall. The remaining portions of the wall of each annular memory cell have a body contact region that serves to elec. connect the annular memory cell to an adjacent **array** well region. The **DRAM** cell **array** also includes a plurality of **word lines** overlaying the vertical **MOSFETs**, and a plurality of bit lines that are orthogonal to the plurality of **word lines**.

L42 ANSWER 3 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:213766 HCAPLUS
DN 136:240125
TI Method of fabricating **wordline** in memory **array** of semiconductor device
IN Chen, Gary; Li, Li; Hu, Yongjun Jeff
PA Micron Technology, Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6358788	B1	20020319	US 1999-385396	19990830
	US 2001003061	A1	20010607	US 2000-738796	20001215
	US 6455906	B2	20020924		
	US 2001050349	A1	20011213	US 2001-864606	20010524
PRAI	US 1999-385396	A3	19990830		

AB Metal nitride and metal oxynitride extrusions often form on metal silicides. These extrusions can cause short circuits and degrade processing yields. The present invention discloses a method of selectively removing such extrusions. In one embodiment, a novel wet etch comprising an oxidizing agent (e.g., H_2O_2) and a chelating agent (e.g., EDTA) selectively removes the extrusions from a **wordline** in a memory **array**. In another embodiment, the wet etch includes a base that adjusts the pH of the etch to selectively remove certain extrusions relative to other substances in the **wordline**. Accordingly new metal silicide structures can be used to form novel **wordlines** and other types of integrated circuits.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L42 ANSWER 4 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:421696 HCAPLUS
TI Vertical gain cell and **array** for a **dynamic random access memory**
IN Noble, Wendell P.
PA Micron Technology, Inc., USA
SO U.S., 20 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6246083	B1	20010612	US 1998-28807	19980224
	US 2001028078	A1	20011011	US 2001-879592	20010612
	US 2001030338	A1	20011018	US 2001-879602	20010612
PRAI	US 1998-28807	A3	19980224		

AB A vertical gain memory cell including an n-channel **metal-oxide semiconductor** field-effect **transistor** (**MOSFET**) and p-channel junction field-effect transistor (JFET) transistors formed in a vertical pillar of semiconductor material is provided. The body portion of the p-channel transistor is coupled to a second source/drain region of the **MOSFET** which serves as the gate for the JFET. The second source/drain region of the **MOSFET** is additionally coupled to a charge storage node. Together the second source/drain region and charge storage node provide a bias to the body of the JFET that varies as a function of the data stored by the memory cell.

A non destructive read operation is achieved. The stored charge is sensed indirectly in that the stored charge modulates the conductivity of the JFET so that the JFET has a first turn-on threshold for a stored logic "1" condition and a second turn-on threshold for a stored logic "0" condition. The charge storage node is a plate capacitor which surrounds the second source/drain region of the **MOSFET**. The vertical gain cell is fabricated so that the write **word line**, read bit line, read **word line** and capacitor are buried beneath the **silicon** surface. As a result the cell can be fabricated in an area as small as four (4) lithographic feature squares.

RE.CNT 133 THERE ARE 133 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L42 ANSWER 5 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:754544 HCAPLUS
DN 133:304550
TI Fabrication of self-isolated and self-aligned 4f-square vertical FET-trench **DRAM** cells
IN Holmes, Steven John; Kalter, Howard Leo; Tiwari, Sandip; Welser, Jeffrey John
PA International Business Machines Corp., USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6137128	A	20001024	US 1998-94383	19980609
PRAI	US 1998-94383		19980609		

AB A densely packed **array** of vertical semiconductor devices, having pillars, deep trench capacitors, vertical transistors, and methods of making thereof are disclosed. The pillars act as transistor channels, and may be formed using the application of hybrid resist over a block of semiconductor material. Drain doped regions are formed on the top of each pillar. The source doped regions and the plate doped regions are self-aligned and are created by diffusion in the trenches surrounding the pillars. The **array** has columns of bitlines and rows of **wordlines**. The capacitors are formed by isolating n+-**polysilicon** in trenches sepg. said pillars. The **array** is suitable for GBit **DRAM** applications because the deep trench capacitors do not increase **array** area. The **array** may have an open bitline architecture, where the plate region is common to all the storage nodes or a folded architecture with two **wordlines** that pass through each cell having stacked transistors, where one **wordline** is active and the other is passing for each cell.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L42 ANSWER 6 OF 24 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:205211 HCAPLUS
DN 132:215644
TI Manufacture of semiconductor memory device
IN Hong, Ki-Gak
PA LG Semicon Co., Ltd., S. Korea
SO Faming Zhuanli Shenqing Gongkai Shuomingshu, 23 pp.
CODEN: CNXXEV
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI CN 1187041	A	19980708	CN 1997-114679	19970716

PRAI CN 1997-114679 19970716
AB The device includes **word lines** and bit lines for connecting the units in unit **array** regions, and a dummy pattern layer on peripheral circuit region of adjacent unit **array** region for decreasing the stage cover between the unit **array** region and the peripheral circuit region.

L42 ANSWER 7 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2003-015985 [01] WPIX
DNN N2003-011917 DNC C2003-003836
TI Compact **dynamic random access memory** cell **array** has annular memory cells including vertical **metal oxide semiconductor** field effect **transistor** and capacitor that are electrically connected through buried-strap out-diffusion region.
DC L03 U11 U12 U13 U14
IN MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 2002105019 A1 20020808 (200301)* 26p
ADT US 2002105019 A1 US 2001-777576 20010205
PRAI US 2001-777576 20010205
AB US2002105019 A UPAB: 20030101
NOVELTY - A compact **dynamic random access memory** cell **array** comprises annular memory cells, each including a vertical **metal oxide semiconductor** field effect **transistor** (**MOSFET**) and a capacitor that are in electrical contact to each other through a buried-strap out-diffusion region. The **array** also includes **wordlines** formed over the **MOSFETs**, and bit lines provided orthogonal to the **wordlines**.

DETAILED DESCRIPTION - A compact **dynamic random access memory** (**DRAM**) cell **array** comprises annular memory cells arranged in rows and columns. Each memory cell includes a vertical **MOSFET** (100) and an underlying capacitor (102) that are in electrical contact to each other through a buried-strap out-diffusion region (24). The buried-strap out-diffusion region is present within a portion of a wall of each annular memory cell such that the portion partially encircles the wall. The remaining portions of the wall of each memory cell have a body contact region (19) that serves to electrically connect the annular memory cell to an adjacent **array** well region (11). The **DRAM** cell **array** also includes **wordlines** (52) provided over the **MOSFETs** and arranged in the row direction, and bit lines (60) provided orthogonal to the **wordlines**.

An INDEPENDENT CLAIM is included for the production of the above compact **DRAM** cell **array**, comprising forming deep trenches in an **array** portion of a **silicon**-containing substrate having a hard mask. The deep trenches are arranged in rows and columns, and include collar oxide regions formed on their walls and a recessed deep trench conductor formed between the collar oxide regions. The buried-strap out-diffusion region is then formed within a portion of the wall. The **MOSFETs**, each having an insulating capping layer, are next formed in the deep trenches above the recessed deep trench conductor. The hard mask abutting the deep trenches is removed to expose sidewall portions of the **MOSFETs**, and diffusion regions are then formed in the substrate. Sidewall masking layers are provided on the diffusion regions to cover the exposed sidewall portions of the **MOSFETs**. Etching is then performed through exposed diffusion

regions and a portion of the substrate not protected by the insulating capping layer and the sidewall masking layers to electrically isolate adjacent buried-strap out-diffusion regions from each other and to form annular active areas adjacent to the deep trenches. A mandrel material is formed in the etched areas and over the insulating cap layer. The **wordlines** are then formed over the **MOSFETs** in the rows.
A portion of the mandrel material between adjacent deep trenches, and bitline contacts (58) are then formed. The bitlines are then formed over the **wordlines**.

USE - As **dynamic random access memory** cell **array**.

ADVANTAGE - The **DRAM** cell **array** has compact cell structure and minimizes floating-body effects and device-to-device interactions.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the vertical **DRAM** cell **array**.

Array well region 11
Body contact region 19
Wordlines 52
Bitline contacts 58
Bit lines 60
MOSFET 100
Capacitor 102
Dwg.1/7

L42 ANSWER 8 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-749260 [81] WPIX
CR 1998-517237 [44]; 2001-089737 [10]
DNN N2002-589974 DNC C2002-212333
TI Semiconductor device production comprises sequentially forming, on substrate, **array** of cells, lower doped regions, gate regions, isolation regions, and upper doped regions.
DC L03 U11 U12 U13 U14
IN FURUKAWA, T; HAKEY, M C; HOLMES, S J; HORAK, D V; KALTER, H L; MANDELMAN, J A; RABIDOUX, P A; WELSER, J J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6440801 B1 20020827 (200281)* 73p
ADT US 6440801 B1 CIP of US 1997-787418 19970122, Div ex US 1998-93928 19980609, US 2000-604901 20000628
FDT US 6440801 B1 CIP of US 5990509, Div ex US 6114725
PRAI US 1998-93928 19980609; US 1997-787418 19970122; US 2000-604901 20000628
AB US 6440801 B UPAB: 20021216

NOVELTY - The production of a semiconductor device comprises forming an **array** of cells having upwardly-extending pillars arranged in rows and columns on a substrate; and sequentially forming lower doped regions below the pillars, gate regions on the pillar sidewalls, isolation regions to isolate each pillar from the gate regions, and upper doped regions on the pillars. The isolation region isolates each pillar from one of the gate regions to prevent one of the gate regions from turning on a pillar device.

USE - For the production of a semiconductor device, e.g. a **metal-oxide semiconductor** field-effect **transistor** for an electrically-erasable programmable read only memory or **dynamic random access memory** application.

ADVANTAGE - The resulting semiconductor device has higher speed and endurance than a conventional floating gate transistor.

DESCRIPTION OF DRAWING(S) - The figure shows an **array** of cells.

Bitlines 220
Wordlines 225, 225'
Bitline direction 314
Dwg.52/78

L42 ANSWER 9 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-416762 [44] WPIX
DNN N2002-327955
TI Sense amplifier for use with a **dynamic random access memory** (**DRAM**), the pitch (lateral size) of the sense amplifiers is made to match the pitch of the smallest memory cells using U-shaped gate design and offset transistor rows.
DC U13 U14
IN LEHMANN, G; LEIDINGER, T; REITH, A M; REITH, A
PA (INFN) INFINEON TECHNOLOGIES AG; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP
CYC 22
PI WO 2002029894 A2 20020411 (200244)* EN 47p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR
US 6404019 B1 20020611 (200244)
ADT WO 2002029894 A2 WO 2001-US27143 20010830; US 6404019 B1 US 2000-676870 20000929
PRAI US 2000-676870 20000929
AB WO 200229894 A UPAB: 20020711
NOVELTY - A sense amplifier is formed in a **silicon** integrated circuit. The pitch of an **array** of such amplifiers is equal to the pitch of pairs of bit lines (150) of a memory **array**. Each **array** of amplifiers is formed from four rows of transistors of an n or p- channel type **MOS** transistor with a U-shaped gate electrode. The gate electrode of the transistors in each row of transistors of the amplifier is offset from those in a previous row by a pre-selected amount. The bit lines are straight.
USE - With **dynamic random access memory** fabricated in semiconductor integrated circuits
ADVANTAGE - Allows support circuits, such as sense amplifiers, to be designed with a width commensurate with the width of the memory cells, has a simple repetitive structure, cost effective, does not introduce extra capacitance onto the bit lines
DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a prior art memory circuit which can be used in conjunction with the invention.
Memory cells 110
Top **array** 120
Bottom **array** 130
Word lines 140
Bit lines 150
Dwg.1/8

L42 ANSWER 10 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2002-280051 [32] WPIX
DNN N2002-218702 DNC C2002-082311
TI Nonvolatile memory cell, e.g. non volatile random access memory, has vertical electrical via which couples plate of capacitor through insulator layer to gate of transistor.
DC L03 U11 U13
IN CLOUD, E H; NOBLE, W P
PA (CLOU-I) CLOUD E H; (NOBL-I) NOBLE W P; (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 2002024083 A1 20020228 (200232)* 20p
US 6380581 B1 20020430 (200235)

01/21/2003

ADT US 2002024083 A1 US 1999-259493 19990226; US 6380581 B1 US 1999-259493 19990226

PRAI US 1999-259493 19990226

AB US2002024083 A UPAB: 20020521

NOVELTY - Nonvolatile memory cell (200A-200B) comprises transistor (210A-210B), a capacitor (220A-220B), and a vertical electrical via (230A-230B). The via couples a first plate (223) of the capacitor through an insulator layer (232) to gate (212A-212B) of the transistor.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(I) a non volatile memory **array** (200) comprising the above-mentioned non volatile memory cells, a **wordline** coupled to the top plate of the stacked capacitor, a bit line (219A-219B) coupled to a drain region (216A-216B) of **metal oxide semiconductor** field effect **transistor** (**MOSFET**), and a sourceline (217A-217B) coupled to a source region (215A-215B) of the **MOSFET**;

(II) an electronic system comprising a processor, a **dynamic random access memory** (**DRAM**) chip, and a system bus coupling the processor to the **DRAM** chip;

(III) a method for forming a non volatile memory cell on a **DRAM** chip comprising forming a **MOSFET** in a substrate on the **DRAM** chip, forming a stacked capacitor above the gate of the **MOSFET** using a **DRAM** process, and forming an electrical contact using a **DRAM** process;

(IV) a method of operating a memory cell comprising controlling a charge on the gate of **MOSFET** and on the bottom plate of the capacitor to regulate a threshold voltage for the memory cell; and

(V) a method of programming a memory device comprising grounding a source region for **MOSFET**, applying a control gate voltage to the top plate, and applying a drain voltage of approximately half of the control gate voltage to a drain region of the **MOSFET**.

USE - Used as non volatile access memory, e.g. electrically erasable and programmable read only memory, or a flash memory cell (claimed).

ADVANTAGE - Operates with lower programming voltages than that used by conventional non volatile memory cells, yet still hold sufficient charge to withstand the effects of parasitic capacitances and noise due to circuit operation, thus realizing the requirements of low power density packed integrated circuits for smaller, portable devices.

DESCRIPTION OF DRAWING(S) - The drawing shows a perspective view of a non volatile memory **array**.

memory **array** 200

nonvolatile memory cell 200A-200B

transistor 210A-210B

gate 212A-212B

source region 215A-215B

drain region 216A-216B

sourceline 217A-217B

bit line 219A-219B

capacitor 220A-220B

plate 223

electrical via 230A-230B

insulator layer 232

Dwg.2/8

L42 ANSWER 11 OF 24 WPIX (C) 2003 THOMSON DERWENT

AN 2002-254581 [30] WPIX

DNN N2002-196658

TI Gain cell for **dynamic random access memory**, has read bit line and read **word line** coupled to different transistors which are formed on vertical pillar.

DC U13 U14

01/21/2003

IN NOBLE, W P
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 2001028078 A1 20011011 (200230)* 19p
ADT US 2001028078 A1 Div ex US 1998-28807 19980224, US 2001-879592 20010612
FDT US 2001028078 A1 Div ex US 6246083
PRAI US 1998-28807 19980224; US 2001-879592 20010612
AB US2001028078 A UPAB: 20020513

NOVELTY - Source/drain region (32) and gate of the transistor (26) are coupled with a write bit line (60) and a write **word line** (65), respectively. An intermediate region (36) of the transistor (26) comprising a source/drain region (82) of a p-channel JFET (28) is coupled with a read bit line (90). A read **word line** (95) is coupled with source/drain region (84) of the transistor (28) whose gate (88) is provided in the source/drain region (34).

DETAILED DESCRIPTION - The gain cell has a vertical pillar (120) with multiple sides extending from a substrate (130). A charge storage node (110) surrounds a portion of the pillar adjacent to source/drain region (34) of n-channel **MOSFET** (26). INDEPENDENT CLAIMS are also included for the following:

(a) Memory cell **array**;
(b) Data storage device;
(c) Gain memory cell reading method;
(d) Gain cell fabrication method;
(e) Gain memory cell **array** fabrication method

USE - For semiconductor memory devices such as **dynamic random access memory.**

ADVANTAGE - The transistors occupy less surface area on the **silicon** chip. The gain cell provides increased cell density and is fabricated in an area as small as four lithographic features. The fabricated gain memory cell provides non-destructive read operations and increased capacitance for greater data retention times.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a gain cell.

n-channel **MOSFET** 26
p-channel JFET 28
Source/drain regions 32,34,82,84
Intermediate region 36
Write bit line 60
Write **word line** 65
Gate 88
Read bit line 90
Read **word line** 95
Charge storage node 110
Vertical pillar 120
Substrate 130
Dwg.3/4

L42 ANSWER 12 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2000-564709 [52] WPIX
CR 2000-096429 [08]; 2001-089623 [43]
DNN N2000-417038 DNC C2000-168182
TI Fabrication of **dynamic random access memory** involves forming gate oxides of different thickness.
DC L03 U11 U13
IN CHANG, K; LU, N C
PA (ETRO-N) ETRON TECHNOLOGY INC
CYC 1
PI US 6107134 A 20000822 (200052)* 12p
ADT US 6107134 A Div ex US 1998-84409 19980526, US 1999-431134 19991101
PRAI US 1998-84409 19980526; US 1999-431134 19991101

01/21/2003

AB US 6107134 A UPAB: 20010224
NOVELTY - A **dynamic random access memory** (**DRAM**) is fabricated upon a semiconductor substrate by forming a gate oxide of first thickness, masking a first set of areas on the substrate, and forming a gate oxide of second thickness.
DETAILED DESCRIPTION - Fabrication of **DRAM** upon a semiconductor substrate (10) involves forming gate oxide (90) of first thickness upon the substrate. A first set of areas on the substrate is masked. It includes sense amplifiers, row address buffers, **word line** decoders, column address buffers, column address decoders, and timing and control circuits. A gate oxide (110) of second thickness is formed by forming at least one gate oxide with a first thickness upon the substrate in a second set of areas. The second set of areas includes **array** of **DRAM** cells, **word line** drivers, boost voltage circuits, and input/output circuits.
USE - For fabricating **DRAM** upon a semiconductor substrate.
ADVANTAGE - The method provides a **DRAM** device having improved performance of peripheral circuitry by having **metal oxide semiconductor** (**MOS**) **transistors** with a thinner gate oxide in circuits having a lower voltage. It also provides a **DRAM** device having improved reliability of each memory cells and selected peripheral sub-circuitry subjected to a higher voltage having thicker gate oxide.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of semiconductor substrate illustrating the method of forming gate oxide having multiple thickness.
Substrate 10
Gate oxide 90, 110
Dwg.4f/5

L42 ANSWER 13 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 2000-022392 [02] WPIX
DNN N2000-016610
TI **Dynamic random access memory** (**DRAM**).
DC U13 U14
IN SHIRLEY, B
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5986946 A 19991116 (200002)* 10p
ADT US 5986946 A US 1996-692950 19960807
PRAI US 1996-692950 19960807
AB US 5986946 A UPAB: 20000112
NOVELTY - Pull-down **MOS** transistors (Q100,Q200) are connected to the ends of **wordlines** (35-0 to 35-255) of an interleaved row **array** memory (38). The gates of the transistors are coupled to a universal phase signal input to a decoder circuit. The transistors terminals are connected to conductive and supply lines. Based on a control signal from control terminals, the conductive lines of respective transistors are connected to the supply line.
DETAILED DESCRIPTION - The decoder circuit is connected to the drain of one transistor at one end of a **wordline**. The other transistor has its drain connected to the other end of the **wordline**. The conductive line consists of a **polysilicon wordline**. An INDEPENDENT CLAIM is also included for a method of driving a **wordline** in a **DRAM**.
USE - None given.
ADVANTAGE - Simplifies construction and layout, as space occupied by the chip is less. Reduces row shut-off time.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the interleaved row **array DRAM**.

Interleaved row **array** memory 38
Wordlines 35-0 to 35-255
Pull-down **MOS** transistors Q100,Q200
Dwg.4/6

L42 ANSWER 14 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1999-443759 [37] WPIX
CR 2000-364286 [31]
DNN N1999-330979 DNC C1999-130642
TI High density **dynamic random access memory** (**DRAM**) **array** with relaxed metal pitch.
DC L03 U11 U14
IN LU, J; KIRSCH, H C; LU, C
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 2
PI US 5933725 A 19990803 (199937)* 15p
TW 452940 A 20010901 (200240)
ADT US 5933725 A US 1998-85612 19980527; TW 452940 A TW 1999-106584 19990421
PRAI US 1998-85612 19980527
AB US 5933725 A UPAB: 20020626

NOVELTY - The **DRAM array** has **polysilicon word lines** and overlying metal conductor lines separated by an insulating layer. The **polysilicon** lines are connected to the conductor lines by through holes and metal plugs at intervals along their length. In this way the overall resistance of the **word line** is reduced. The method also allows for relaxation in minimum design rules for metal spacing.

DETAILED DESCRIPTION - Method of stitching **polysilicon word lines** of a memory cell **array** to conductive metal lines by; (a) Forming an **array** of memory cells on a **silicon** wafer having **MOSFET** devices, a number of **polysilicon word lines**, bit lines, lower insulative layers, and storage capacitors. (b) Forming and planarizing an insulative layer over the wafer. (c) Depositing and patterning a photoresist layer to define first contact openings to each of the **word lines**. (d) Etching the first and lower insulative layer to form contact openings. (e) Removing the photoresist and depositing a first metal over the wafer and into the openings. (f) Depositing and patterning a second photoresist to define an alternating sequence of first line segments and gap parallel to and along the length of the **word lines**, each of the line segments extending over at least two sequential contact openings, and each of the gaps extending between two or more contact openings and the alternating sequence is reversed in phase between next adjacent **word lines** such that first line gaps become line segments and vice versa. (g) Etching the first metal layer to form first metal line segments connected to the **polysilicon word lines** by metal in the contact openings and zero or more metal plugs in the first line gaps. (h) Removing the photoresist and depositing and globally planarizing a second insulative layer. (i) Depositing and patterning a third photoresist to define second contact openings at each end of the first metal line segment. (j) Etching second contact openings through the insulative layer to expose parts of the end portions of the first metal line segments and first metal plugs in the first line gaps. (k) Removing the photoresist, depositing a second metal layer. (l) Depositing and patterning a fourth photoresist to define and alternating sequence of second line segments and second line gaps parallel to and along the length of the **polysilicon word lines** with each of the segments overlapping sequential subjacent first line segments. (m) Etching the second metal layer to form a pattern of second line segments sequentially connecting the ends of the first line segments through metal

plugs to form a set of parallel conductive bands each alternating along its length between two conductive layers and stitched to a subjacent **word line**. (n) Removing the photoresist.

USE - **DRAM** and other memory **arrays**

ADVANTAGE - The overall resistance of the **word line** is reduced for improved speed, and method also allows for relaxation in minimum design rules for metal spacing.

DESCRIPTION OF DRAWING(S) - The drawings show a **DRAM** **array** including; cross section direction 8
row decoders 16, 18
silicon wafer 40
field oxide 42
bit line 44
word line 46
rectangular section storage capacitors 62
insulator 64
strap 70
tungsten strap 72
interlevel contact 76
aluminum layer 78
tungsten plug 79
insulating layer 82
Dwg.7,11/14

L42 ANSWER 15 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1999-343772 [29] WPIX
CR 1995-071855 [10]
DNN N1999-258291 DNC C1999-101425
TI **MOS** transistor manufacture for stack type **DRAM** - involves forming first metal wiring for fleshing **word line** of memory and second metal wiring thicker than first wiring for peripheral circuit of memory, patterned conductive layer.
DC L03 U11 U12 U13 U14
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 11126887 A 19990511 (199929)* 12p
ADT JP 11126887 A Div ex JP 1994-68365 19940406, JP 1998-225706 19940406
PRAI JP 1993-86084 19930413
AB JP 11126887 A UPAB: 19990723

NOVELTY - Surface of electrically conductive layer (67) smoothed by surface polishing, to obtain a predetermined pattern. Metal wiring (57) for fleshing **word line** of memory and wiring (58) thicker than the wiring (57) are formed on the patterned conductive layer. The wiring (57) is formed at a position higher than that of wiring (58).

DETAILED DESCRIPTION - A memory cell **array** area, **silicon** dioxide film (59) and electrically conductive layer (67) are sequentially laminated on a semiconductor substrate (53).

USE - For stack type **DRAM**.

ADVANTAGE - Enables to arrange height of upper surface of wiring, even when thickness of wiring is changed.

DESCRIPTION OF DRAWING - The figure shows **MOS** transistor manufacturing process. (53) Semiconductor substrate; (57) Metal wiring; (58) Wiring; (59) **Silicon** dioxide film; (67) Conductive layer.
Dwg.3/9

L42 ANSWER 16 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1999-180221 [15] WPIX
CR 2000-159839 [12]
DNN N1999-132377
TI Memory circuit for e.g. **DRAM** with reduced size by use of small sub-**word line** driver circuit.

01/21/2003

DC U13 U14
IN CHUNG, J; KIM, J; OH, J
PA (HYUN-N) HYUNDAI ELECTRONICS AMERICA
CYC 1
PI US 5875149 A 19990223 (199915)* 14p
ADT US 5875149 A US 1997-828817 19970206
PRAI US 1997-828817 19970206
AB US 5875149 A UPAB: 20000320

NOVELTY - The gate terminal of a **NMOS** pull down transistor of the inverters in each sub-**word line** is connected to the respective global **word line**. The source and drain terminals of the pull down transistor is connected to the **MOS** transistor. The turn ON/OFF time of the **MOS** transistor is controlled according to state switching of signals on the global and sub-**word lines**.

DETAILED DESCRIPTION - The memory cells (204) are arranged in the matrix shape. Sub-**word line** drivers (210) are connected between the respective global **word lines** (GWL) and sub- **word lines** (SWL). The row address information is decoded and passed to the global **word line** by a row decoder (202). The signal on the global **word line** is inverted by the pull down transistors. A resistor is also connected to the pull down transistor.

USE - For e.g. **DRAM**.

ADVANTAGE - Reduces memory size by using small sub-**word line** driver circuit. Eliminates need for routing of second complementary global **word line** across **array**. Improves operating speed of memory by reducing power consumption. Avoids need for **PMOS** transistors for sub-**word line** driver circuit. Improves density of memory **array** by driving **polysilicon** sub-**word lines** by single global metal **word line**.

DESCRIPTION OF DRAWING(S) - The figure shows partial schematic diagram of memory **array**.

Row decoder 202
Memory cells 204
Sub-**word line** driver 210
Dwg.2/8

L42 ANSWER 17 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1998-427037 [36] WPIX
CR 1999-370537 [31]
DNN N1998-333316 DNC C1998-128693
TI Forming an external contact to a **MOSFET** of a stacked capacitor **DRAM** for testing - by forming an opening in the upper cell plate of the cells capacitor and contacting the storage plate through the opening with a conductive plug..
DC L03 U11 U12 U13 U14
IN HUANG, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 5783462 A 19980721 (199836)* 8p
ADT US 5783462 A US 1997-787195 19970122
PRAI US 1997-787195 19970122
AB US 5783462 A UPAB: 19990806

A method of forming an external electrical contact to the **MOSFET** drain of a stacked capacitor **DRAM** cell comprises: (a) forming a **silicon** wafer (10) having; (i) a **MOSFET** formed within its surface; (ii) a **polysilicon wordline** (16) forming the gate of the **MOSFET**; (iii) a **polysilicon** bitline (20) connected to the source of the **MOSFET**; (iv) a capacitor

storage plate (19) connected to the drain of the **MOSFET**; (b) depositing a layer of dielectric material over the wafer; (c) depositing a doped **polysilicon** layer over the dielectric material; (d) depositing and patterning a first photoresist layer to define a first opening in the doped **polysilicon** layer over the storage plate; (e) etching the doped **polysilicon** layer and the layer of dielectric material to form the first opening in the doped **polysilicon** layer and the layer of dielectric material thereby exposing the capacitor storage plate; (f) removing the first photoresist layer; (g) depositing an insulative layer; (h) planarising the insulative layer; (i) depositing and patterning a second photoresist layer; (j) etching the insulative layer to form a second opening smaller than, and concentric with the first opening, exposing the capacitor storage plate; (k) removing the second photoresist layer; (1) forming a conductive plug (66) in the second opening; (m) depositing a metal layer; (n) depositing and patterning a third photoresist layer; (o) etching the metal layer to form a metal stripe connected to the conductive plug; (p) removing the third photoresist layer; (q) providing a device for connecting electrical test instrumentation to the **polysilicon wordline**, the **polysilicon** bitline, the **silicon** wafer and the metal stripe. A method for measuring the threshold voltage of a **MOSFET** in a stacked capacitor **DRAM** test cell **MOSFET** is also claimed.

USE - For making external contact to a **MOSFET** drain for testing stacked capacitor **DRAMs**.

ADVANTAGE - The test structures can be built at any position in the **array** and the metal connection lines for the contacts do not interfere with the structure of the test **array** itself other than the test cell form the **array**. Multiple devices may be designated from anywhere in the **array** and probe contacts may be conveniently located on the chip.

Dwg.4/6

L42 ANSWER 18 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1995-060339 [08] WPIX
DNN N1995-048010 DNC C1995-026873
TI Forming closely spaced capacitors on **DRAM** chips - between bottom electrodes to increase capacitor area and capacitance.
DC L03 U11 U13 U14
IN HONG, G; HSUE, C
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 5380675 A 19950110 (199508)* 10p
ADT US 5380675 A US 1994-210933 19940321
PRAI US 1994-210933 19940321
AB US 5380675 A UPAB: 19950301

A method of making an **array** of closely spaced storage capacitors over a semiconductor substrate (18) having an **array** of device regions, **word lines** and bit lines, comprises depositing an insulating layer (42) to isolate the lines and a second, different, insulating layer (44) to form a diffusion barrier. Openings are made to device contacts, a **poly-Si** layer deposited (46), and a third insulating layer (48) forming a diffusion barrier to oxidn. is formed and etched to give exposed **poly-Si** areas. This **poly-Si** is thermally and partly oxidised, the third insulating layer removed, and the **poly-Si** selectively etched to leave a closely spaced **array** of isolated bottom capacitor electrodes. Oxidised regions are removed from these electrodes and a capacitor dielectric layer (52) formed. A second **poly-Si** layer is then deposited to form the top electrode to complete the stacked capacitor **array** aligned to and

contacting the device regions. Also claimed is a method as above in which an **array** of **DRAM** cells is formed with an **array** of **MOSFETs** under the stacked storage capacitors above.

USE - For storage capacitors in **DRAM** chips in VLSI.

ADVANTAGE - The narrow spacing extends the current photolithographic resolution limit and increases capacitance, which is further augmented by roughening the bottom electrode and using a high dielectric insulator.
Dwg.6/6

L42 ANSWER 19 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1990-046091 [07] WPIX
DNN N1990-035389 DNC C1990-020029
TI CMOS one-capacitor **DRAM** - uses non-boosted **word line** without suffering threshold loss.
DC L03 U13 U14
IN DHONG, S H; HENKELS, W H; LU, N C C; LU, N C
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 14
PI EP 354348 A 19900214 (199007)* EN 9p
R: CH DE ES FR GB IT LI NL SE
JP 02068792 A 19900308 (199016)
US 4910709 A 19900320 (199017)
US 4927779 A 19900522 (199024)
CN 1040462 A 19900314 (199050)
CA 1314991 C 19930323 (199317)
KR 9211046 B1 19921226 (199415)
ADT EP 354348 A EP 1989-112325 19890706; JP 02068792 A JP 1989-184889 19890719; US 4910709 A US 1988-230410 19880810; US 4927779 A US 1989-428159 19891027; CA 1314991 C CA 1989-600744 19890525; KR 9211046 B1 KR 1989-9780 19890710
PRAI US 1988-230410 19880810
AB EP 354348 A UPAB: 19930928
A memory cell structure (8) for a dynamic semiconductor **array**, operating with a non-boosted **wordline** and without a threshold loss problem, and having pairs of **wordlines** (26, 28) for transmitting signals, each at two signal levels, comprises an MNOS (18) and a **PMOS** (12) device, both including first and second gate electrodes, and a storage capacitor (30). The first electrodes of the transistors are connected to a bit line (34) of the memory **array**, and the second electrodes to the capacitor (30). The **NMOS** and CMOS gate electrodes (18, 20) are connected to the first and second **wordlines** (26, 28) respectively, and the transistors are turned off by the first signal level on the **wordlines** and on at the second signal level. The bit line is connected to the capacitor, charge being stored into and read out from the capacitor in response to the turning on and off of the transistors.

USE/ADVANTAGE - A CMOS one-capacitor **DRAM** and method of fabrication are provided, the cell operating with a non-boosted **wordline** but without suffering from the threshold loss problem. Thus the area of the **DRAM** cells may be reduced.
1/5

L42 ANSWER 20 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1988-176633 [26] WPIX
DNN N1988-135019
TI High density **VMOS** dynamic RAM **array** - has trench capacitor, and single access transistor with gate connected to **word line** and drain connected to bit line.
DC U11 U13 U14
IN HWANG, W; SCHUSTER, S E; TERMAN, L; TERMAN, L M
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP

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CYC  6
PI   EP 272476     A  19880629 (198826)* EN   11p
         R: DE FR GB IT
     JP 63157463   A  19880630 (198832)
     US 4763180    A  19880809 (198834)        9p
     EP 272476     B1 19930407 (199314)  EN   15p
         R: DE FR GB IT
     DE 3785317    G  19930513 (199320)
ADT  EP 272476 A EP 1987-117303 19871124; JP 63157463 A JP 1987-259877
     19871016; US 4763180 A US 1986-945275 19861222; EP 272476 B1 EP
     1987-117303 19871124; DE 3785317 G DE 1987-3785317 19871124, EP
     1987-117303 19871124
FDT  DE 3785317 G Based on EP 272476
PRAI US 1986-945275    19861222
AB   EP    272476 A UPAB: 19930923
```

The semiconductor memory storage cell has a semiconductor substrate (10), and at least two laterally spaced vertical trenches in the substrate. The trenches are filled with doped **polysilicon** material (16). Conductive material (22,18,54,58) is disposed between each trench to form a conductive path between the doped **polysilicon** in each trench.

A layer (26,56) of epitaxial material is deposited over the substrate covering at least the conductive material (22,54) between the trenches. An insulator coated V-shaped groove provides a gate oxide which separates the conductive material between the trenches and the **polysilicon** filled trenches into separate storage capacitors. The doped layer region (30) on the epitaxial layer is separated into bit lines (BL).

ADVANTAGE - **Array** needs only single level of **polysilicon** and has no contacts.

1/14

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L42  ANSWER 21 OF 24  WPIX (C) 2003 THOMSON DERWENT
AN   1986-280259 [43]   WPIX
DNN  N1986-209444
TI   Dynamic RAM with capacitor transistor memory cells - has semiconductor
     layers of opposed conductivity type vertically stacked on groove walls.
DC   U13 U14
IN   WADA, M
PA   (TOKE) TOSHIBA KK
CYC  6
PI   EP 198590     A  19861022 (198643)* EN   17p
         R: DE FR GB
     JP 61239658   A  19861024 (198649)
     KR 9001225    B  19900305 (199103)
     US 4990980    A  19910205 (199108)
     US 5001078    A  19910319 (199114)
     EP 198590     B1 19920520 (199221)  EN   23p
         R: DE FR GB
     DE 3685361    G  19920625 (199227)
     US 5504028    A  19960402 (199619)       14p
ADT  EP 198590 A EP 1986-301758 19860311; JP 61239658 A JP 1985-80619 19850416;
     US 4990980 A US 1989-390510 19890807; US 5001078 A US 1989-389417
     19890804; EP 198590 B1 EP 1986-301758 19860311; DE 3685361 G DE
     1986-3685361 19860311, EP 1986-301758 19860311; US 5504028 A Cont of US
     1986-837881 19860310, Cont of US 1989-390510 19890807, Cont of US
     1990-584102 19900918, Div ex US 1994-361173 19941221, US 1995-464385
     19950605
FDT  DE 3685361 G Based on EP 198590; US 5504028 A Cont of US 4990980
PRAI JP 1985-80619    19850416
AB   EP    198590 A UPAB: 19930922
```

A p+ **silicon** substrate is provided with a number of grooves to define island layers. Cell capacitors are formed by an electrode layer

insulatively buried at the bottom of a groove, and n- type layers formed in the lower side surfaces of the grooves.

Cell transistors are formed by a gate electrode region insulatively stacked in the groove above the capacitor electrode layer. Transistor p-type channel regions are formed on the u-ppupper part of the groove side walls, drain layers being formed on the upper surface of the islands.

ADVANTAGE - Memory cell packing density is increased without decreasing capacitance of memory capacitors.

2/7

L42 ANSWER 22 OF 24 WPIX (C) 2003 THOMSON DERWENT
AN 1983-766300 [38] WPIX
CR 1985-082577 [14]; 1985-321477 [51]
DNN N1994-255185
TI High density integration semiconductor memory with trench capacitor - has capacitor formed on side walls of an island region surrounded with recess formed in **silicon** substrate used as major part of electrode surface of capacitor.
DC U11 U12 U13 U14
IN KAWAMOTO, Y; KURE, T; MIYAO, M; SUNAMI, H; TAMURA, M
PA (HITA) HITACHI LTD
CYC 9
PI EP 88451 A 19830914 (198338)* EN 76p
R: DE FR GB
JP 58154256 A 19830913 (198342)
US 4751557 A 19880614 (198826)
EP 88451 B 19880810 (198832) EN
R: DE FR GB
DE 3377687 G 19880915 (198838)
US 4984030 A 19910108 (199105)
JP 03268357 A 19911129 (199203)
KR 9007606 B 19901017 (199203)
US 5357131 A 19941018 (199441)B 62p
ADT EP 88451 A EP 1983-102371 19830310; US 4751557 A US 1986-904397 19860908; US 4984030 A US 1988-201100 19880531; US 5357131 A Cont of US 1983-474002 19830310, CIP of US 1984-654459 19840926, Cont of US 1985-726978 19850425, Div ex US 1986-904397 19860908, CIP of US 1988-180770 19880412, Div ex US 1988-201100 19880531, CIP of US 1991-636720 19910102, Cont of US 1991-753944 19910903, US 1993-93033 19930719
FDT US 5357131 A Div ex US 4751557, Div ex US 4984030
PRAI JP 1982-36418 19820310; JP 1991-25993 ; JP 1983-177952 19830928; JP 1983-246948 19831228; JP 1984-81750 19840425
AB US 5357131 A UPAB: 19941206 ABEQ treated as Basic
Semiconductor memory includes capacitors which are information storage portions, and insulated-gate field effect transistors which read out signal charges in the information storage portions. Part of each capacitor is formed on side walls of an island region which is surrounded with a recess provided in a surface region of a semiconductor substrate. The island region is electrically isolated from other regions of the semiconductor substrate by the recess.

A number of recesses are formed to provide a number of the islands, and the number of recesses are respectively formed by the use of oxide regions spaced apart from one another. The oxide regions used to form the recesses include oxide mask regions and field oxide regions. The oxide mask regions and the field oxide regions alternate with one another at the surface region of the semiconductor substrate, and a pitch between the recesses is equal to one half of a pitch between the oxide mask regions.

USE/ADVANTAGE - Semiconductor memory which requires small area and exhibits high density of integration, n-channel and p-channel **MOSFET**, single transistor **DRAM**.

49,50/106

AB EP 88451 A UPAB: 19941212
The information storage regions of the memory are formed by the capacitors. A part of each capacitor is formed on side walls of an island region which is surrounded by the recess (17) provided in a surface region of the semiconductor substrate (10). The recess provides isolation for the active regions of the memory cells. By dispensing with the need for an isolating field oxide film, which has been used in the prior art, the area required to implement the memory is significantly reduced.
Signal charges stored in the capacitor are read-out by respective insulated-gate field-effect transistors (4, 15) formed in the surface region of the semiconductor substrate. The respective capacitor includes an insulating film (12) and a plate electrode (8) formed on the side walls of the island region.
7/6
Dwg.7/6

L42 ANSWER 23 OF 24 JAPIO COPYRIGHT 2003 JPO
AN 1999-354739 JAPIO
TI SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE
IN SATO WATARU
PA TOSHIBA CORP
PI JP 11354739 A 19991224 Heisei
AI JP 1998-157091 (JP10157091 Heisei) 19980605
PRAI JP 1998-157091 19980605
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a **DRAM** hybrid LSI capable of improving mass productivity by using constant processing conditions without depending upon the scale of a **DRAM**.
SOLUTION: Trench capacitors 20 are arrayed and formed onto a **silicon** substrate under the state, in which upper sections are covered with insulating films. **MOS** transistors 40 constituting memory cells together with the trench capacitors 20 are formed by utilizing a part of a region, in which the trench capacitors 20 are arrayed and formed. Gates for the **MOS** transistors 40 are formed in continuously disposed **word lines** WL, and bit lines BL connected to sources for the **MOS** transistors 40 are crossed with the **word lines** and arranged. A **MOS** transistor 50 configuring a peripheral circuit is formed in a region in which the trench capacitors 20 are buried, on the outside of a **DRAM** cell **array** under the state in which the **MOS** transistor 50 is insulated from the trench capacitors 20.
COPYRIGHT: (C)1999,JPO

L42 ANSWER 24 OF 24 JAPIO COPYRIGHT 2003 JPO
AN 1999-251545 JAPIO
TI DYNAMIC SEMICONDUCTOR STORAGE DEVICE
IN AKITA HIRONOBU
PA TOSHIBA CORP
PI JP 11251545 A 19990917 Heisei
AI JP 1998-46439 (JP10046439 Heisei) 19980227
PRAI JP 1998-46439 19980227
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a dynamic semiconductor storage device(**DRAM**) which enables potential change of a plate electrode to be restrained, ensuring read operation margin, and high speed access.
SOLUTION: A memory cell 2 constituted of an **MOS** transistor QM and a capacitor C, a **word line** constituted of a gate electrode 14 of the **MOS** transistor QM, and a bit line 16 are formed on a **silicon** substrate 11, and a memory cell **array** is constituted. A capacitor C is constituted of a storage node 18 formed on an interlayer insulating film 17, and a plate electrode

01/21/2003

20 as a common electrode which is formed on the storage node 18 via a capacitor insulating film 19. The plate electrode 20 is brought directly into contact with a diffused layer 22 of an **MOS** transistor Q2 the layer of which is a power source terminal layer of a bit line recharging circuit 3, via a contact hole 24 and is used as a precharge power source.

01/21/2003

L56 ANSWER 1 OF 18 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:5143 HCAPLUS
TI Modified vertical **MOSFET** and methods of formation thereof
IN **Divakaruni, Ramachandra**; Dev, Prakash C.; Malik, Rajeev; Nesbit, Larry
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003001200	A1	20030102	US 2001-896741	20010629
	DE 10226569	A1	20030116	DE 2002-10226569	20020614
PRAI	US 2001-896741	A	20010629		

AB The vertical **MOSFET** structure used in forming **dynamic random access memory** comprises a gate stack structure comprising one or more **silicon** nitride spacers; a vertical gate **polysilicon** region disposed in an array trench, wherein the vertical gate **polysilicon** region comprises one or more **silicon** nitride spacers; a bitline diffusion region; a shallow trench isolation region bordering the array trench; and wherein the gate stack structure is disposed on the vertical gate **polysilicon** region such that the **silicon** nitride spacers of the gate stack structure and vertical gate **polysilicon** region form a borderless contact with both the bitline diffusion region and shallow trench isolation region. The vertical gate **polysilicon** is isolated from both the bitline diffusion and shallow trench isolation region by the nitride spacer, which provides reduced bitline capacitance and reduced incidence of bitline diffusion to vertical gate shorts.

L56 ANSWER 2 OF 18 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:941860 HCAPLUS
DN 138:10456
TI Method for novel SOI **DRAM** BICMOS NPN
IN **Divakaruni, Ramachandra**; Houghton, Russell J.; Mandelman, Jack A.; Pricer, W. David; Tonti, William R.
PA International Business Machines Corporation, USA
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6492211	B1	20021210	US 2000-656819	20000907
PRAI	US 2000-656819		20000907		

AB There is disclosed herein a unique fabrication sequence and the structure of a vertical Si on insulator (SOI) bipolar transistor integrated into a typical **DRAM** trench process sequence. A **DRAM** array using an NFET allows for an integrated bipolar NPN sequence. Similarly, a vertical bipolar PNP device is implemented by changing the array transistor to a PFET. Particularly, a BICMOS device is fabricated in SOI. The bipolar emitter contacts and CMOS diffusion contacts are formed simultaneously of **polysilicon** plugs. The CMOS diffusion contact is the plug contact from bitline to storage node of a memory cell.
RE.CNT 23 THERE ARE 23 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L56 ANSWER 3 OF 18 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:425255 HCAPLUS
TI Embedded vertical **dram** cells and dual workfunction logic gates
IN Gruening, Ulrike; **Divakaruni, Ramachandra; Mandelman, Jack**; Rupp, Thomas
PA Infineon Technologies North America Corp., USA; International Business Machines Corporation
SO PCT Int. Appl.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002045130	A2	20020606	WO 2001-US44625	20011128

W: CN, JP, KR
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR

PRAI US 2000-725412 A 20001129
AB A process for producing very high-density embedded **DRAM**/very high-performance logic structures comprising fabricating vertical **MOSFET DRAM** cells with salicided source/drain and **gate conductor** dual workfunction **MOSFETs** in the supports.

L56 ANSWER 4 OF 18 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:592218 HCAPLUS
DN 135:145762
TI Method of forming bitline diffusion halo under **gate conductor** ledge of **MOSFET** for **DRAM** to improve threshold voltage control
IN Mandelman, Jack A.; **Divakaruni, Ramachandra**; Tonti, William R.
PA International Business Machines Corp., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6274441	B1	20010814	US 2000-560073	20000427

PRAI US 2000-560073 20000427
AB A method for fabricating a **MOSFET** device including a halo implant comprising providing a semiconductor substrate, a gate insulator layer, a conductor layer, an overlying silicide layer, and an insulating cap; patterning and etching the silicide layer and the insulating cap; providing insulating spacers along sides of said silicide layer and insulating cap; implanting node and bitline N+ diffusion regions; patterning a photoresist layer to protect the node diffusion region and supporting PFET source and drain regions and expose the bitline diffusion region and NFET source and drain regions; etching exposed spacer material from the side of said silicide layer and insulating cap; implanting a P-type impurity halo implant into the exposed bitline diffusion region and supporting NFET source and drain regions; and stripping the photoresist layer and providing an insulating spacer along the exposed side of said silicide layer and insulating cap.
RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L56 ANSWER 5 OF 18 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:553341 HCAPLUS

01/21/2003

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DN   133:128765
TI   Field-shield-trench isolation for trench capacitor DRAM
IN   Mandelman, Jack A.; Larosa, Giuseppe; Radens, Carl; Divakaruni,
     Rama; Gruening, Ulrike
PA   Infineon Technologies North America Corp., USA; International Business
     Machines Corp.
SO   Eur. Pat. Appl., 17 pp.
     CODEN: EPXXDW
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE          APPLICATION NO.   DATE
     ---------------   ----  --------      ---------------   --------
PI   EP 1026745         A2   20000809      EP 2000-101131    20000121
         R:  AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,
             IE, SI, LT, LV, FI, RO
     KR 2000057898      A    20000925      KR 2000-5305      20000203
     CN 1267913         A    20000927      CN 2000-104636    20000203
     JP 2000228504      A2   20000815      JP 2000-28340     20000204
     TW 449862          B    20010811      TW 2000-89102368  20000328
PRAI US 1999-245269     A    19990205
AB   A dynamic random access memory (
     DRAM) formed in a semiconductor body has individual pairs of
     memory cells that are isolated from one another by a vertical elec.
     isolation trench and are isolated from support circuitry.  The isolation
     trench has sidewalls and upper and lower portions, and encircles an area
     of the semiconductor body which contains the memory cells.  This elec.
     isolates pairs of memory cells from each other and from the support
     circuitry contained within the semiconductor body but not located within
     the encircled area.  The lower portion of the isolation trench is filled
     with an elec. conductive material that has sidewall portions thereof which
     are at least partly sepd. from the sidewalls of the lower portion of the
     trench by a 1st elec. insulator, and that has a lower portion that is in
     elec. contact with the semiconductor body.  The upper portion of the
     isolation trench is filled with a 2nd elec. insulator.

L56  ANSWER 6 OF 18  HCAPLUS  COPYRIGHT 2003 ACS
AN   2000:481996  HCAPLUS
DN   133:201316
TI   A novel trench DRAM cell with a VERtIcal access transistor and
     BuriEd Strap (VERI BEST) for 4Gb/16Gb
AU   Gruening, U.; Radens, C. J.; Mandelman, J. A.; Michaelis, A.; Seitz, M.;
     Arnold, N.; Lea, D.; Casarotto, D.; Knorr, A.; Halle, S.; Ivers, T. H.;
     Economikos, L.; Kudelka, S.; Rahn, S.; Tews, H.; Lee, H.; Divakaruni,
     R.; Welser, J. J.; Furukawa, T.; Kanarsky, T. S.; Alsmeier, J.;
     Bronner, G. B.
CS   Infineon Technologies, Corp., Hopewell Junction, NY, 12533, USA
SO   Technical Digest - International Electron Devices Meeting (1999) 25-28
     CODEN: TDIMD5; ISSN: 0163-1918
PB   Institute of Electrical and Electronics Engineers
DT   Journal
LA   English
AB   Results are presented for a novel trench capacitor DRAM cell
     using a vertical access transistor along the storage trench sidewall which
     effectively decouples the gate length from the lithog. ground-rule.  A
     unique feature of this cell is the vertical access transistor in the array
     which is self-aligned to the buried strap connection of the storage trench
     (VERI BEST) and bounded by trench isolation oxide.  The VERI BEST cell
     concept, process and elec. results obtained from 8F2 test cell arrays at
     0.175 .mu.m ground-rules are described in this paper.
RE.CNT  5     THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
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01/21/2003

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L56 ANSWER 7 OF 18 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:66737 HCAPLUS
DN 120:66737
TI The current-carrying corner inherent to trench isolation
AU Bryant, Andres; Haensch, W.; Geissler, S.; **Mandelman, Jack**; Poindexter, D.; Steger, M.
CS IBM, Essex Junction, VT, 05452, USA
SO IEEE Electron Device Letters (1993), 14(8), 412-14
CODEN: EDLEDZ; ISSN: 0741-3106
DT Journal
LA English
AB It is shown how the characteristics of the corner **MOSFET** inherent to trench isolation can be extd. from hardware measurements and how the corner device must be taken into account when extg. **MOSFET** channel characteristics. For NFET's the corner's threshold voltage, substrate sensitivity, and sensitivity to well doping are all smaller than the channel's. The results imply that for low standby power logic applications requiring high performance, it may become necessary to locally control the well doping at the corner. However, the corner's reduced substrate sensitivity and width independence can provide a significant advantage in a **DRAM** cell.

L56 ANSWER 8 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2002-739737 [80] WPIX
DNN N2002-582749
TI Semiconductor device e.g. **DRAM** has contact area within rhomboid shape active region connected to node diffusion for providing contact for stacked capacitor.
DC U11 U12 U13 U14
IN **DIVAKARUNI, R**; MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6455886 B1 20020924 (200280)* 34p
ADT US 6455886 B1 US 2000-636564 20000810
PRAI US 2000-636564 20000810
AB US 6455886 B UPAB: 20021212
NOVELTY - A **MOSFET** formed by a node diffusion (126), a source/drain diffusion and a **gate conductor** (120), has a channel extending in a straight line from the node diffusion to the source/drain diffusion. A contact area within a rhomboid shape active region connected to the node diffusion, provides a contact for a stacked capacitor formed above a surface of a semiconductor substrate and connected to active region.

USE - Semiconductor device e.g. **DRAM**.

ADVANTAGE - The rhomboid shape of the active region, allows a word line pitch to be 2.5 F in the array and a bit line pitch to be 2.5 F, thereby enabling a cell area equal to 5F2 while still providing enough space for capacitor contact to be reliably formed in the active region.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the word lines formed in a nitride layer.

Gate conductor 120
Node diffusion 126
Dwg.18/28

L56 ANSWER 9 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2002-641593 [69] WPIX
CR 2002-626871 [67]; 2003-027928 [02]
DNN N2002-507033 DNC C2002-181170
TI Vertical **metal oxide semiconductor** field

effect **transistor** for forming **dynamic random access memory**, has vertically disposed **gate conductor**, vertically arranged array well, bitline diffusion region, and storage node diffusion region.

DC L03 U11 U12 U13 U14

IN **DIVAKARUNI, R**; LEE, H; MANDELMAN, J A; RADENS, C J; SIM, J

PA (DIVA-I) DIVAKARUNI R; (LEEH-I) LEE H; (MAND-I) MANDELMAN J A; (RADE-I) RADENS C J; (SIMJ-I) SIM J; (IBMC) INT BUSINESS MACHINES CORP

CYC 1

PI US 6414347 B1 20020702 (200269)* 10p
US 2002089007 A1 20020711 (200269)

ADT US 6414347 B1 Div ex US 2001-757514 20010110, US 2001-790011 20010209; US 2002089007 A1 Div ex US 2001-757514 20010110, US 2001-790011 20010209

PRAI US 2001-757514 20010110; US 2001-790011 20010209

AB US 6414347 B UPAB: 20030111

NOVELTY - A vertical **metal oxide semiconductor** field effect **transistor (MOSFET)** comprises a vertically arranged **gate conductor** (14) formed within a recess of a semiconductor substrate; a vertically arranged array well having a top surface and first and second side surfaces; a bitline diffusion (20) region; and a storage node diffusion (22) region

DETAILED DESCRIPTION - A vertical **MOSFET** structure comprises:

(i) a vertically arranged **gate conductor** formed within a recess of a semiconductor substrate;

(ii) a vertically arranged array well having a top surface and first and second side surfaces;

(iii) a bitline diffusion region; and

(iv) a storage node diffusion region formed beneath the bitline diffusion region and adjacent the **gate conductor**.

The first side surface of the array well located adjacent to the **gate conductor** and separated from the conductor by an insulator layer. The bitline further comprises a crescent-shaped diffusion portion, formed in the top surface of the array well. The crescent-shaped diffusion portion has a first boundary terminating before the first side surface of the array well. It further has a second boundary terminating before the second side surface of the array well. A diffusion pocket (30) is formed along a top corner of the array well. The top corner is along an intersection of the top surface and the first side surface of the array well. The diffusion pocket further overlapping the first boundary of the crescent-shaped diffusion portion.

An INDEPENDENT CLAIM is included for a semiconductor memory array structure comprising memory storage cell(s) including a **MOSFET** access transistor and a storage capacitor; a horizontally arranged wordline coupled to a vertically arranged **gate conductor** which is formed within a recess of a semiconductor substrate; a vertically arranged array well; a bitline diffusion region; a storage node diffusion region; and a horizontally arranged bitline.

USE - Used in forming **dynamic random access memories**.

ADVANTAGE - The **MOSFET** has minimized adverse performance and yield impacts. It has reduced gate to top diffusion overlap capacitance, reduced bitline diffusion area, reduced incidence of diffusion to gate shorts (reduced incidence of diffusion stud to **gate conductor** shorts, and improved immunity to backside parasitic conduction.

DESCRIPTION OF DRAWING(S) - The figure is a vertical **MOSFET** structure.

Gate conductor 14
Bitline diffusion 20
Storage node diffusion 22

Pocket 30
Dwg.4/10

L56 ANSWER 10 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2002-626871 [67] WPIX
CR 2002-641593 [69]; 2003-027928 [02]
DNN N2002-495784 DNC C2002-176662
TI Semiconductor **DRAM** memory cell array structure formation involves recessing **gate conductor** below top surface of substrate.
DC L03 U11 U12 U13 U14 V05
IN **DIVAKARUNI, R**; LEE, H; MANDELMAN, J A; RADENS, C J; SIM, J
PA (IBMC) IBM CORP; (DIVA-I) DIVAKARUNI R; (LEEH-I) LEE H; (MAND-I) MANDELMAN J A; (RADE-I) RADENS C J; (SIMJ-I) SIM J
CYC 2
PI US 2002090780 A1 20020711 (200267)* 10p
JP 2002222873 A 20020809 (200267) 8p
ADT US 2002090780 A1 US 2001-757514 20010110; JP 2002222873 A JP 2001-388866 20011221
PRAI US 2001-757514 20010110
AB US2002090780 A UPAB: 20030111
NOVELTY - A recess (34) is formed in a **gate conductor** (22), below the top surface of a substrate. N-type dopant species are implanted through the recess to form doping pockets in the array P-well. A **gate conductor** material is deposited into the recess and the **gate conductor** is planarized to the top surface of trench top oxide (44).

USE - Forming semiconductor **DRAM** cell array structures.

ADVANTAGE - Reduces bitline capacitance, bitline diffusion area, incidence of diffusion to gate shorts and drain induced barrier lowering. Reduces sensitivity of device electrical characteristics to variation in the channel length of the vertical **MOSFET**.

DESCRIPTION OF DRAWING(S) - The figure illustrates the vertical **MOSFET** forming process.

Gate conductor 22
Recess 34
Trench top oxide 44
Dwg.10/10

L56 ANSWER 11 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2002-402626 [43] WPIX
DNN N2002-315758
TI Deep trench capacitor for **MOSFET** use in **DRAM**, has notches formed on trench above N+ capacitor plates positioned in **silicon** substrate at bottom of trench.
DC U12 U13 U14
IN **DIVAKARUNI, R**; KIM, B Y; MANDELMAN, J A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6373086 B1 20020416 (200243)* 19p
ADT US 6373086 B1 US 2000-607135 20000629
PRAI US 2000-607135 20000629
AB US 6373086 B UPAB: 20020709
NOVELTY - The capacitor has notch (30) formed on a trench (26) above a pair of N+ capacitor plates (12,14) that are positioned in a **silicon** substrate at a bottom portion of the trench. A N+ strap (10) and shallow trench isolation (22) are formed adjacent to the trench. Polycrystalline **silicon** (18) is provided within the trench, covered with oxide coatings.

USE - For vertical parasitic **metal oxide semiconductor** field effect **transistor** (**MOSFET**)

used in **DRAM**.
ADVANTAGE - Increases the threshold voltage of the vertical parasitic **MOSFET** between the N+ strap and the N+ plates significantly by providing notch above the plates and the electrical thickness of a gate dielectric is effectively thicker than its actual physical thickness, thereby a reduced amount of gate dielectric and dopant is needed for suppression of vertical parasitic **MOSFET** conduction and the current leakage of vertical parasitic **MOSFET** is suppressed.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the deep trench capacitor.
N+ strap 10
N+ capacitor plates 12,14
Polycrystalline **silicon** 18
Shallow trench isolation 22
Trench 26
Notch 30
Dwg.1/15

L56 ANSWER 12 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2002-375767 [41] WPIX
DNN N2002-293719
TI Semiconductor device manufacturing method e.g. for **DRAM**, involves forming **silicon** layer on side wall of trench and dielectric collar is formed on **silicon** layer.
DC U11 U13
IN **DIVAKARUNI, R**; GRUENING, U; MANDELMAN, J A; RADENS, C J; SUDO, A
PA (IBMC) IBM CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 3
PI JP 2002026148 A 20020125 (200241)* 9p
US 6376324 B1 20020423 (200241)
KR 2002000523 A 20020105 (200244)
ADT JP 2002026148 A JP 2001-189096 20010622; US 6376324 B1 US 2000-602969 20000623; KR 2002000523 A KR 2001-35829 20010622
PRAI US 2000-602969 20000623
AB JP2002026148 A UPAB: 20020701
NOVELTY - An oxidation barrier layer is formed on side wall (15) of the trench in the substrate (14). A photoresist layer is filled in the trench and a specific portion of the photoresist and barrier layers are removed to expose the side wall of the trench. The **silicon** layer is formed on the exposed side wall. A dielectric collar (22) is then formed on the **silicon** layer.
USE - For manufacturing semiconductor device such as **dynamic random access memory**.
ADVANTAGE - The distance between **MOSFET** gate and memory capacitor is increased, hence the biasing of tap portion of the trench is reduced without affecting the memory capacity and the infringement of the diffusion is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of the semiconductor device.
Substrate 14
Side wall 15
Dielectric collar 22
Dwg.3/23

L56 ANSWER 13 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2002-371334 [40] WPIX
DNN N2002-290176
TI Strucure for 6F2 trench capacitor **DRAM** cell with vertical **MOSFET** and 3F bitline pitch, a bitline extends above the substrate and has contact to a source diffusion between shallow trench isolation

regions.

DC U14

IN **DIVAKARUNI, R**; GRUENING, U; MANDELMAN, J A; RADENS, C J

PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP

CYC 22

PI WO 2002001567 A2 20020103 (200240)* EN 42p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR
JP 2002026147 A 20020125 (200240) 20p
US 6339241 B1 20020115 (200240)
KR 2002001569 A 20020109 (200245)
US 2002085434 A1 20020704 (200247)

ADT WO 2002001567 A2 WO 2001-US20221 20010625; JP 2002026147 A JP 2001-189079 20010622; US 6339241 B1 US 2000-602426 20000623; KR 2002001569 A KR 2001-35771 20010622; US 2002085434 A1 Div ex US 2000-602426 20000623, US 2002-11556 20020222

FDT US 2002085434 A1 Div ex US 6339241

PRAI US 2000-602426 20000623; US 2002-11556 20020222

AB WO 200201567 A UPAB: 20020626
NOVELTY - A deep trench in a substrate has a storage capacitor at the bottom. A vertical transistor extends down the trench above the capacitor with a source diffusion by the trench. An isolation extends down opposite the vertical transistor. Shallow trench isolation regions (STI) extend along the substrate surface across the wall with the vertical transistor. A wordline extends over the trench connected to a **gate conductor**. A bitline is connected to the source diffusion.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a process for forming a memory cell structure

USE - In **DRAM** technology

ADVANTAGE - Addresses manufacturing and operational problems associated with smaller and denser memory cell structures

DESCRIPTION OF DRAWING(S) - The drawing shows an overhead view of one embodiment of a memory array according to the invention.

Bitline contact CB

Shallow trench isolation regions STI

Wordlines WL

Dwg.1/10

L56 ANSWER 14 OF 18 WPIX (C) 2003 THOMSON DERWENT

AN 2002-253256 [30] WPIX

DNN N2002-195367 DNC C2002-075768

TI **Metal oxide semiconductor** field effect **transistor** fabrication method for **dynamic random access memory**, involves implanting boron halo implants into bitline diffusion region after etching spacer material.

DC L03 U11

IN **DIVAKARUNI, R**; MANDELMAN, J A; TONTI, W R

PA (IBMC) INT BUSINESS MACHINES CORP

CYC 1

PI US 6274441 B1 20010814 (200230)* 11p

ADT US 6274441 B1 US 2000-560073 20000427

PRAI US 2000-560073 20000427

AB US 6274441 B UPAB: 20020513
NOVELTY - Arsenic silicate glass spacers (34) are placed along sides of patterned silicide layer (28) and nitride cap. Exposed portion of **polysilicon** layer (30) is etched, and node and bitline diffusion regions (38, 40) are implanted. Boron halo implants (48) are implanted into region (40) after etching spacer material. Insulating spacers are provided along exposed sides of silicide layer and nitride cap.

USE - The method is used for fabricating **metal**

oxide semiconductor field effect **transistor** (
MOSFET) used in **dynamic random access**
memory (**DRAM**) cell.
ADVANTAGE - Array threshold voltage control is improved without increasing node diffusion leakage. Hence stored charge is increased and threshold voltage tolerance is improved. Thus process complexity and manufacturing cost are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows **MOSFET** fabrication process.
Silicide layer 28
Polysilicon layer 30
Arsenic silicate glass spacer 34
Bitline diffusion regions 38, 40
Boron halo implant 48
Dwg.6/9

L56 ANSWER 15 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2002-237131 [29] WPIX
DNN N2002-182410 DNC C2002-071765
TI Vertical transistor manufacture for **dynamic random access memory** cell, involves removing portion of conductor under wordline trough and forming wordlines in wordline trough connected to separate **gate conductors**.
DC L03 U11 U12 U13
IN ATHAVALE, S D; BRONNER, G B; **DIVAKARUNI, R**; GRUENING, U; MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6348374 B1 20020219 (200229)* 27p
ADT US 6348374 B1 US 2000-597887 20000619
PRAI US 2000-597887 20000619
AB US 6348374 B UPAB: 20020508
NOVELTY - Trough above bit line is filled with conductor (120). The conductor is cut along longitudinal axis such that conductor remains on one side of trough. Wordline troughs are formed orthogonal to bit line above substrate. A portion of conductor is removed under wordline trough, to separate the conductors. Wordlines are formed in the wordline trough connected to the separate **gate conductors**.
DETAILED DESCRIPTION - The trough is formed in the semiconductor substrate through the pad layer. A bit line is enclosed by a dielectric material. A strap is formed to connect the bit line to substrate.
USE - For **dynamic random access memory** (**DRAM**) cell.
ADVANTAGE - The dynamic coupling effect between the adjacent **metal oxide semiconductor** field effect **transistors** (**MOSFETs**) is reduced.
DESCRIPTION OF DRAWING(S) - The figures show the views of **gate conductors**.
Conductor 120
7, 12/40

L56 ANSWER 16 OF 18 WPIX (C) 2003 THOMSON DERWENT
AN 2001-211373 [21] WPIX
DNN N2001-150999 DNC C2001-062925
TI Disposable doped glass spacers for **MOSFET** gate structure used in high density **DRAMs** or embedded memories are fabricated through modified gate processing, giving improved.
DC L03 U11
IN AKATSU, H; **DIVAKARUNI, R**; LEE, G Y
PA (INFN) INFINEON TECHNOLOGIES CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP

CYC 22
PI WO 2001017010 A1 20010308 (200121)* EN 16p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN JP KR
US 6281084 B1 20010828 (200151)
ADT WO 2001017010 A1 WO 2000-US23850 20000830; US 6281084 B1 US 1999-386832 19990831
PRAI US 1999-386832 19990831
AB WO 200117010 A UPAB: 20010910
NOVELTY - Forming a **gate conductor** (20) for a semiconductor device (10) comprises: providing a substrate with a gate stack (12) including a sidewall; forming dielectric spacers, having inner and outer spacers, on the sidewalls; implanting ions; and removing the outer spacer.
USE - For high density **DRAM** or embedded memories.
ADVANTAGE - Improves gapfill in arrays.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the semiconductor device.
semiconductor device 10
gate stack 12
gate conductor 20
Dwg.1/5

L56 ANSWER 17 OF 18 JAPIO COPYRIGHT 2003 JPO
AN 2002-026147 JAPIO
TI STRUCTURE AND PROCESS FOR 6F2 TRENCH CAPACITOR **DRAM** CELL HAVING VERTICAL **MOSFET** AND 3F BIT LINE PITCH
IN **MANDELMAN JACK** A; RAMACHANDORA DEIVAKARUNI; KAARU JIEI RADENSU; GRUENING ULRIKE
PA INTERNATL BUSINESS MACH CORP <IBM>
PI JP 2002026147 A 20020125 Heisei
AI JP 2001-189079 (JP2001189079 Heisei) 20010622
PRAI US 2000-602426 20000623
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide a memory cell structure including a planar semiconductor substrate.
SOLUTION: The semiconductor substrate has a deep trench. The deep trench has side walls and one bottom part. A storage capacitor is located at the bottom of the deep trench. On at least one sidewall of the deep trench, a vertical transistor extends downwardly. This transistor has source diffusion extending in the plane of the substrate adjacent to the deep trench. On at least the other sidewall of the deep trench on the opposite side from the vertical transistor, a separation part extends downwardly. A shallow trench separation area extends laterally to the sidewall, where the vertical transistor extends along the surface of the substrate. In the inside of the deep trench, a **gate conductor** extends. A word line extends onto the deep trench and is connected to the **gate conductor**. The bit line extends onto the surface of the substrate and has a contact for the source diffusion between shallow trench separation areas.
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L56 ANSWER 18 OF 18 JAPIO COPYRIGHT 2003 JPO
AN 2000-323684 JAPIO
TI MANUFACTURE OF **DYNAMIC RANDOM ACCESS MEMORY**
IN GRUENING ULRIKE; HALLE SCOTT; **RADENS CARL** J; JEFFREY J WERSER; BEINTNER JOCHEN; **MANDELMAN JACK** A; WITTMANN JUERGEN
PA INFINEON TECHNOL NORTH AMERICA CORP
INTERNATL BUSINESS MACH CORP <IBM>

01/21/2003

PI JP 2000323684 A 20001124 Heisei
AI JP 2000-85406 (JP2000085406 Heisei) 20000324
PRAI US 1999-275337 19990324
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To form a trench capacitor in a semiconductor body.
SOLUTION: A trench capacitor 10 and a **MOS** transistor 9 are provided in a substrate 16 to form a cell 8 of the **DRAM**, and the cell 8 is separated from adjacent cells by an STI region 28. The capacitor 10 is composed of an insulator 14 enveloping the trench and a first electrode 24 filled with **polysilicon** 12, is connected to the drain portion 72 through a buried electrode 22, and is insulated from a gate electrode 20 by a dielectric 23. A second electrode 25 is formed in its bottom portion through an insulator 14. A transistor 9 has N-type drain 72 and source 71 in an upper active region 11 of the substrate 16 and operates with a p well as channel.